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MS-7B45

ATX
Ver: 20

Intel -Kabylake plamform Z370

CPU: Coffee Lake-S
System Chipset: Z370

Onboard Chip:
HD Audio Codec:ALC1220
LAN:INTEL I219
SIO:Nuvoton 6795
Flash ROM: SPI 128MB

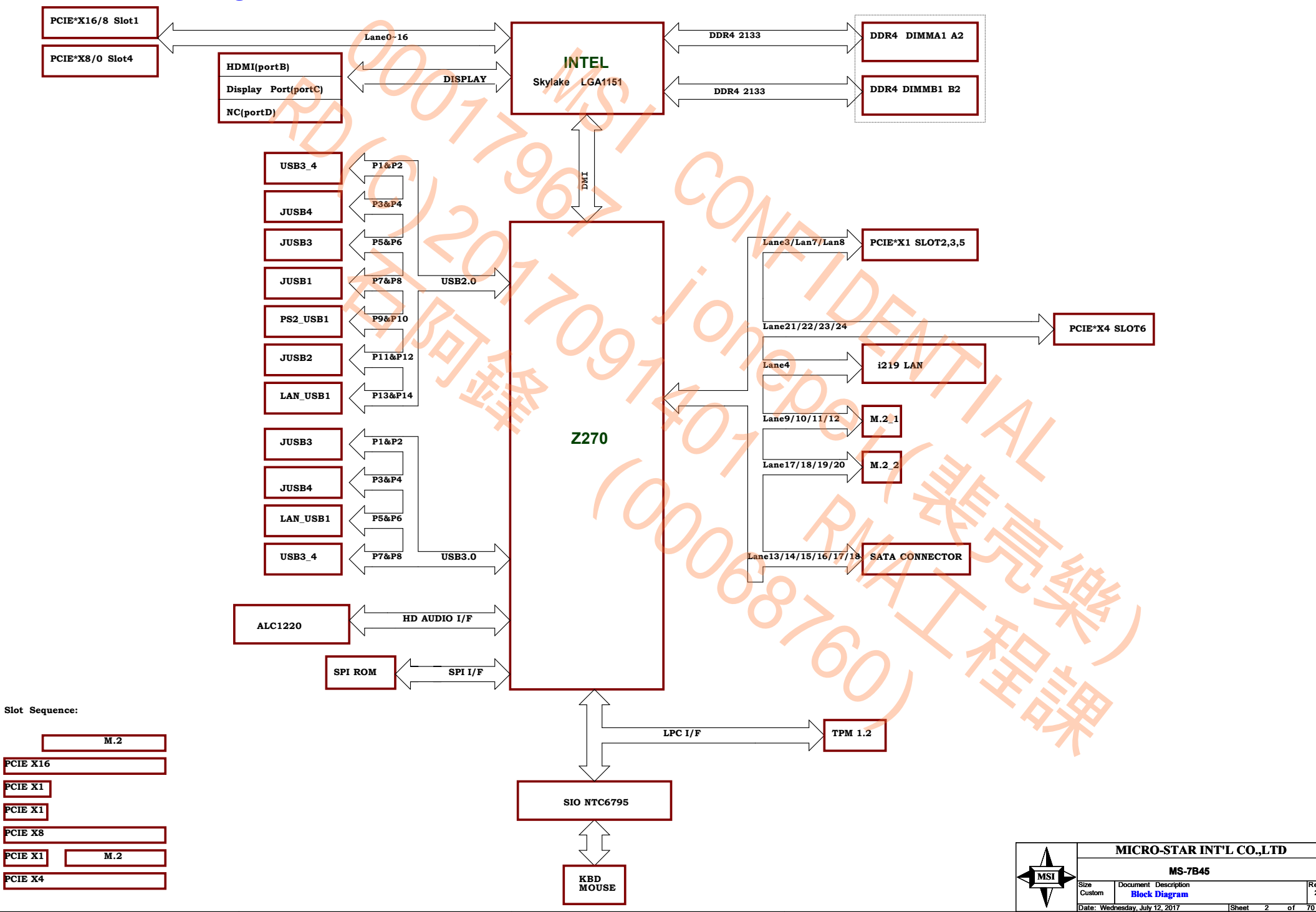
Main Memory:
DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)

ACPI: NIKO/UPI
PWM: UPI9508

Expansion Slots: PCI Express (X16) Slot *1
PCI Express (X8) Slot *1
PCI Express (X4) Slot * 1
PCI Express (X1) Slot * 3
M2 * 2

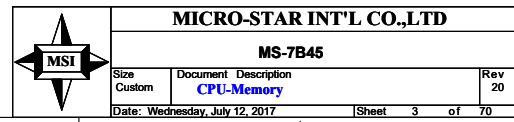
Other: SATA3.0 x6 (PCH)
FRONT USB2.0 *4
FRONTUSB3.0 *4
REAR USB3.0 *4
REAR USB2.0 *2
REAR USB TYPE A+C

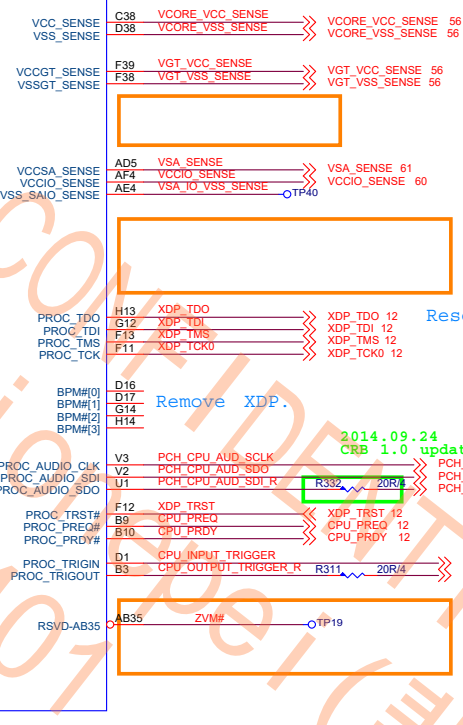
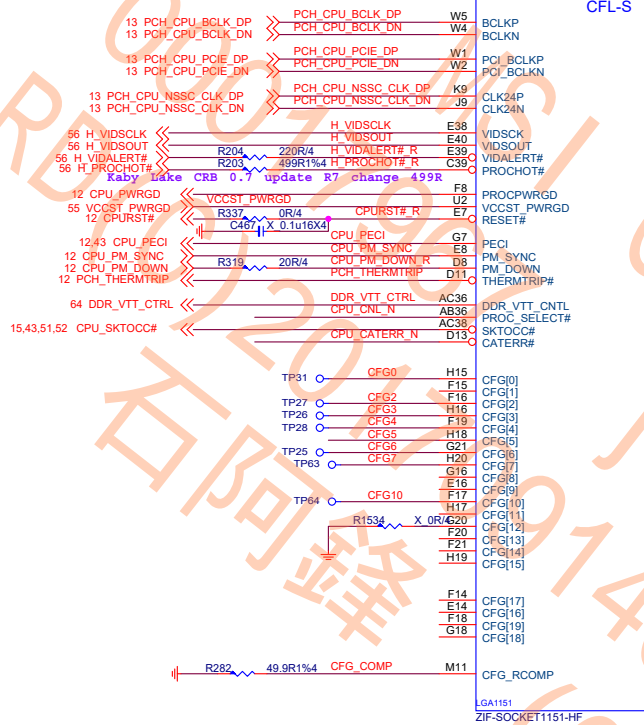
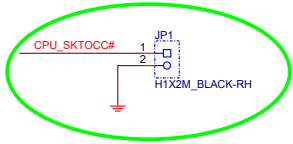
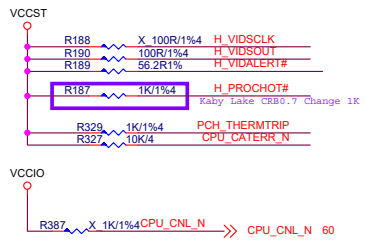
MS-7A63 Block Diagram



Slot Sequence:

M.2
PCIe X16
PCIe X1
PCIe X1
PCIe X8
PCIe X1
M.2
PCIe X4

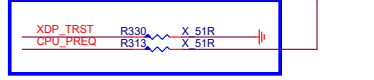
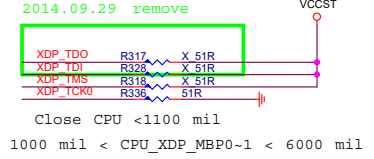




CFG Strap

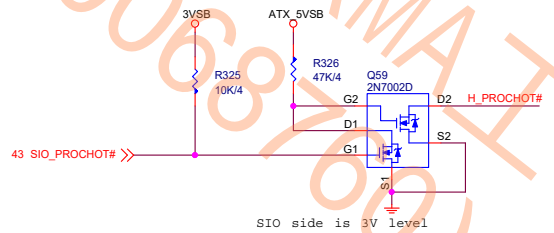
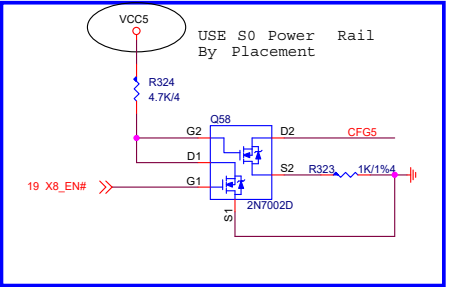
CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEGCPGSEL[0]
6	DISABLE	ENABLE	PEGCPGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		RSVD
15	RSVD		RSVD

Reserve for DCI.



X8 Ctrl

ENABLE#	SLOT1	SLOT4
X8		
0	X8	X8
1	X16	X0



CFG Strap

CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEGCPGSEL[0]
6	DISABLE	ENABLE	PEGCPGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		RSVD
15	RSVD		RSVD

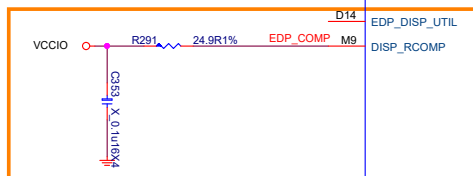
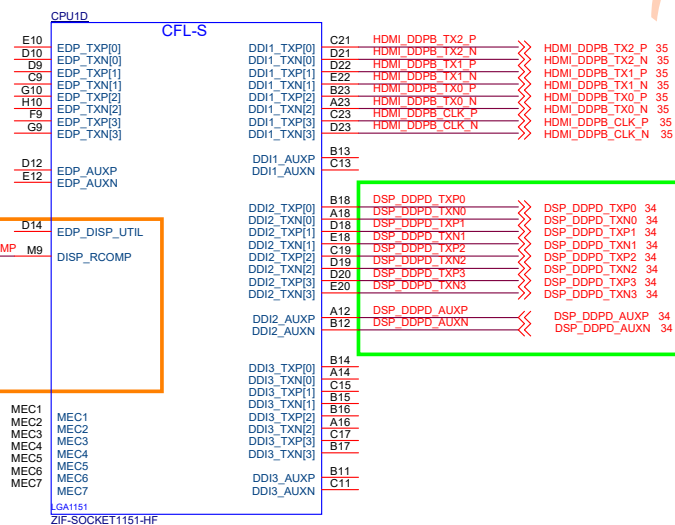
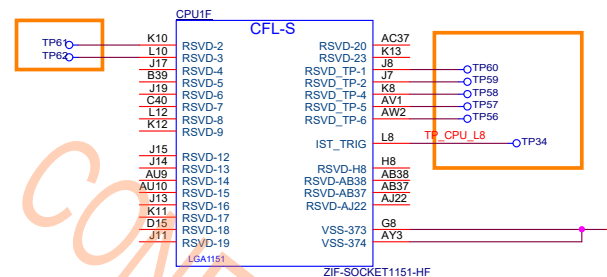
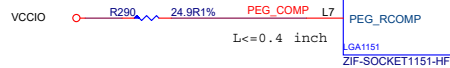
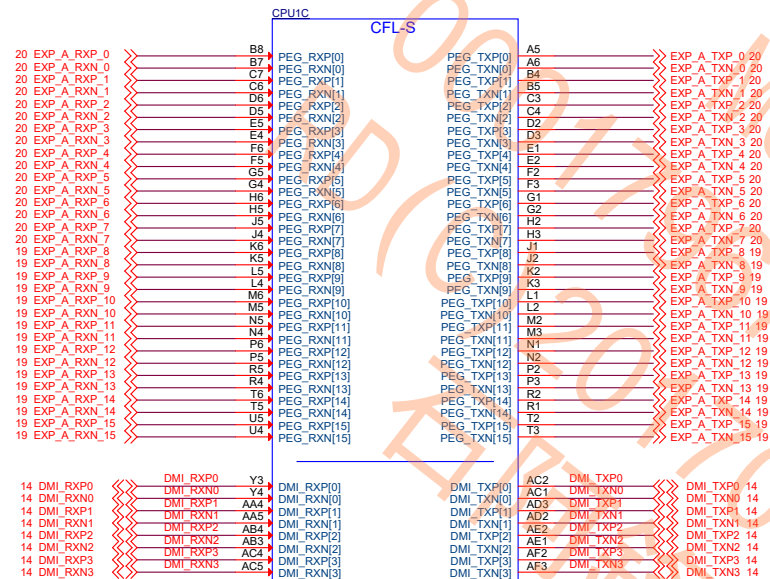
MICRO-STAR INT'L CO.,LTD

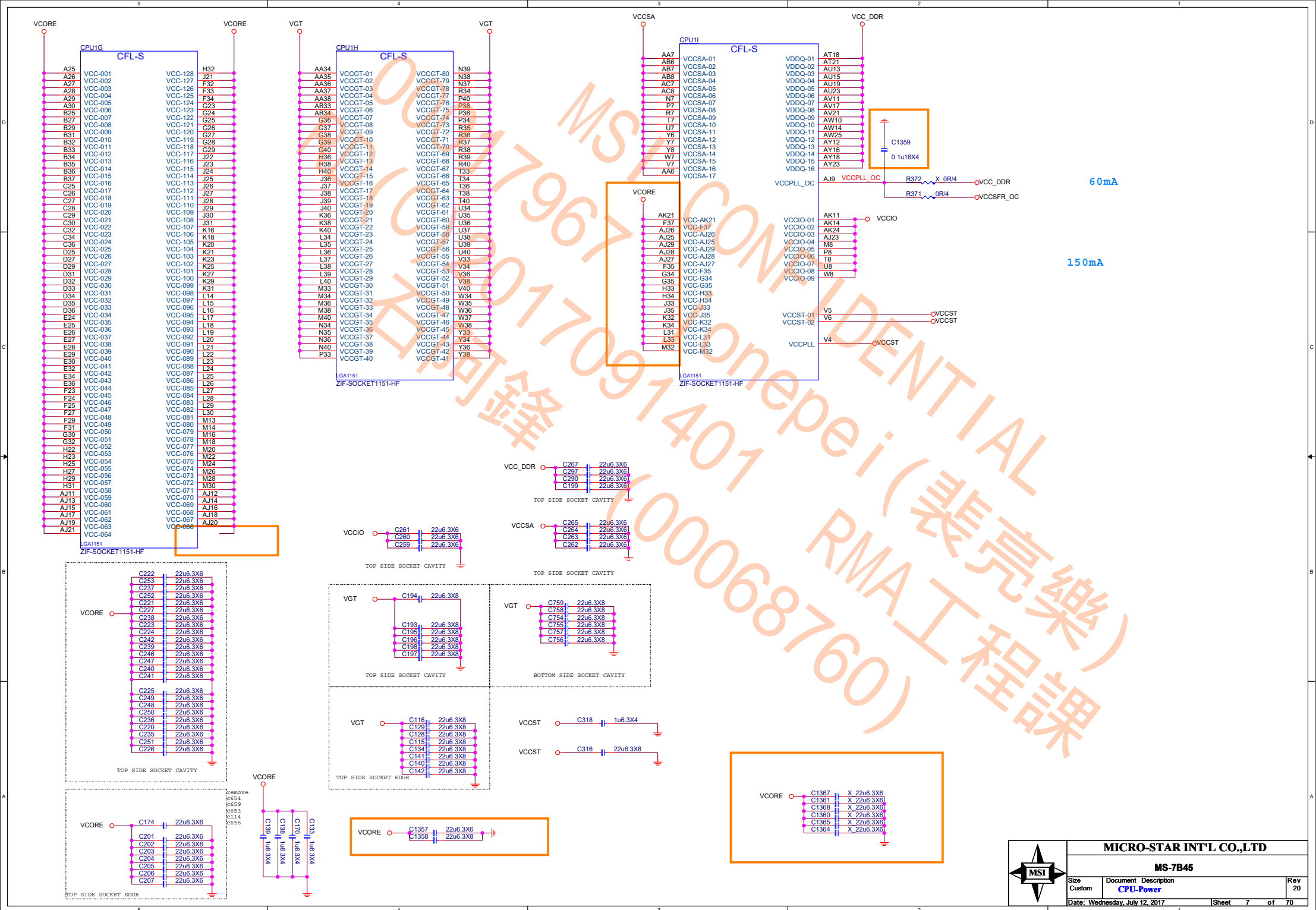
MS-7B45

Size	Document	Description	Rev
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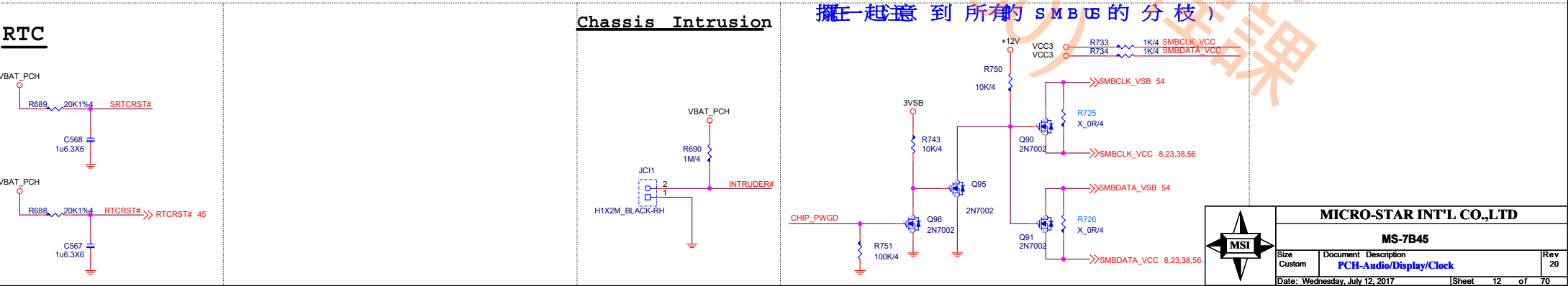
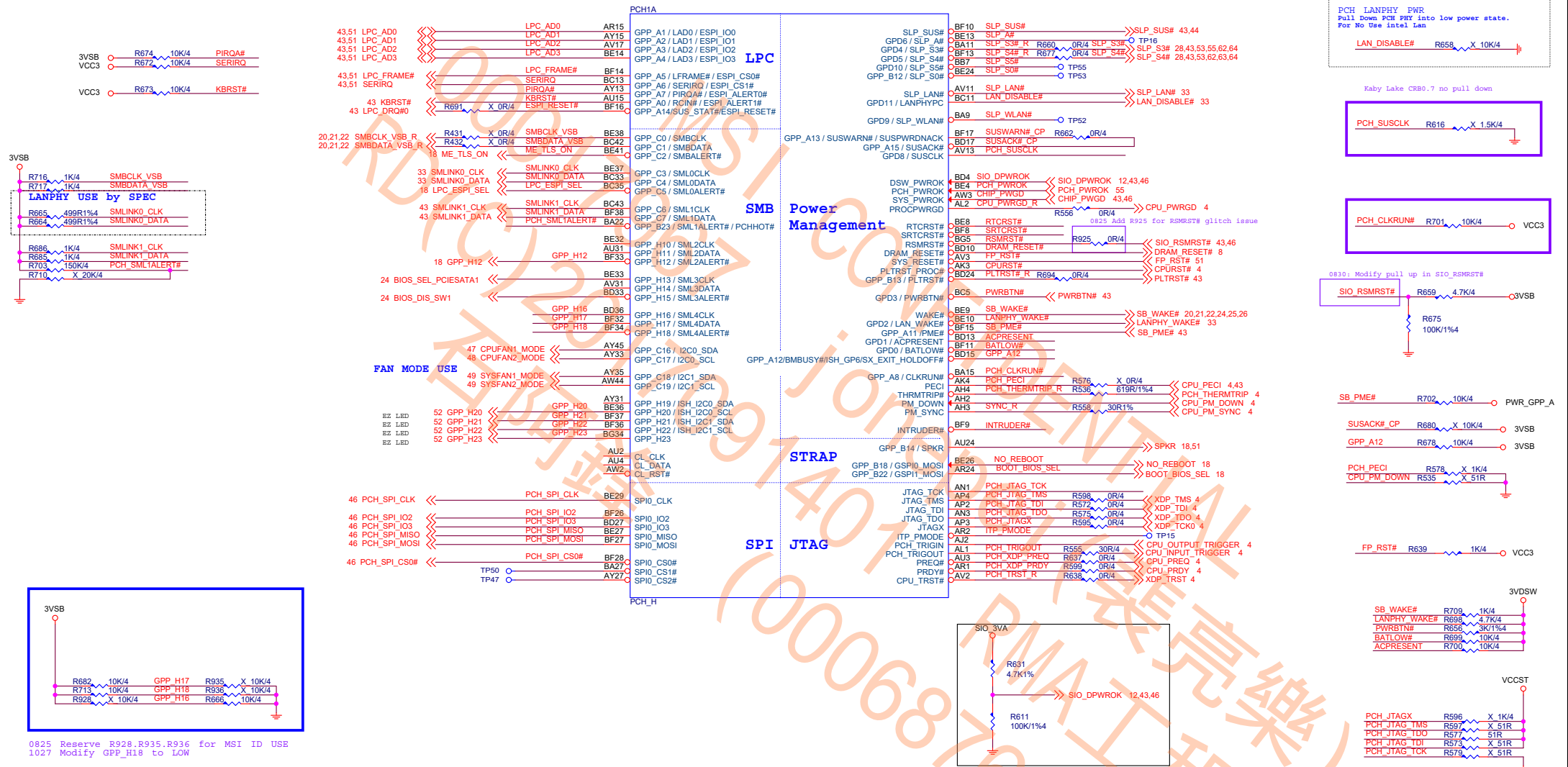
Sheet 4 of 70







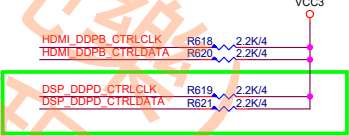
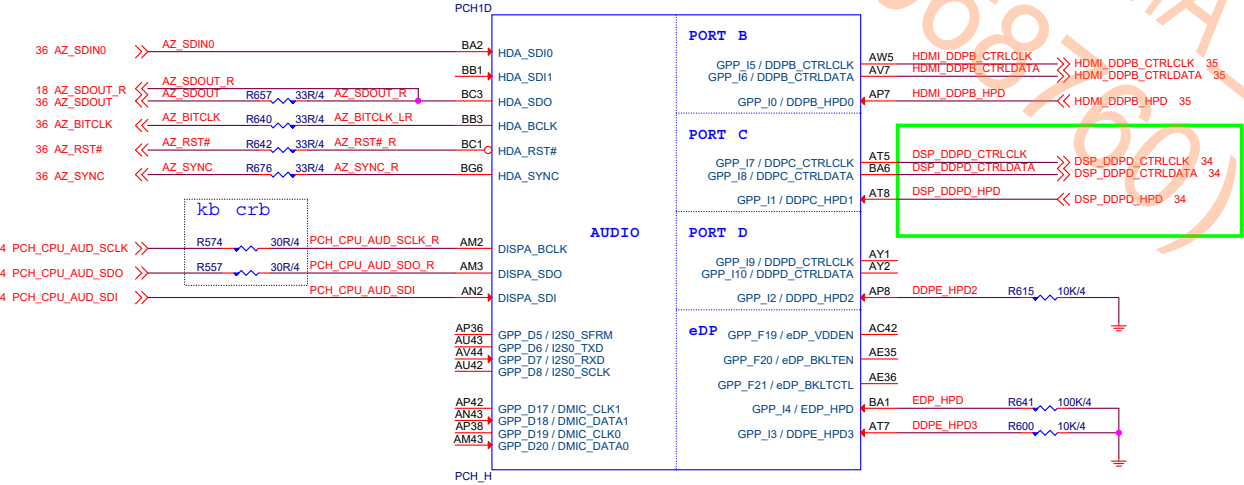
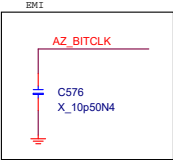
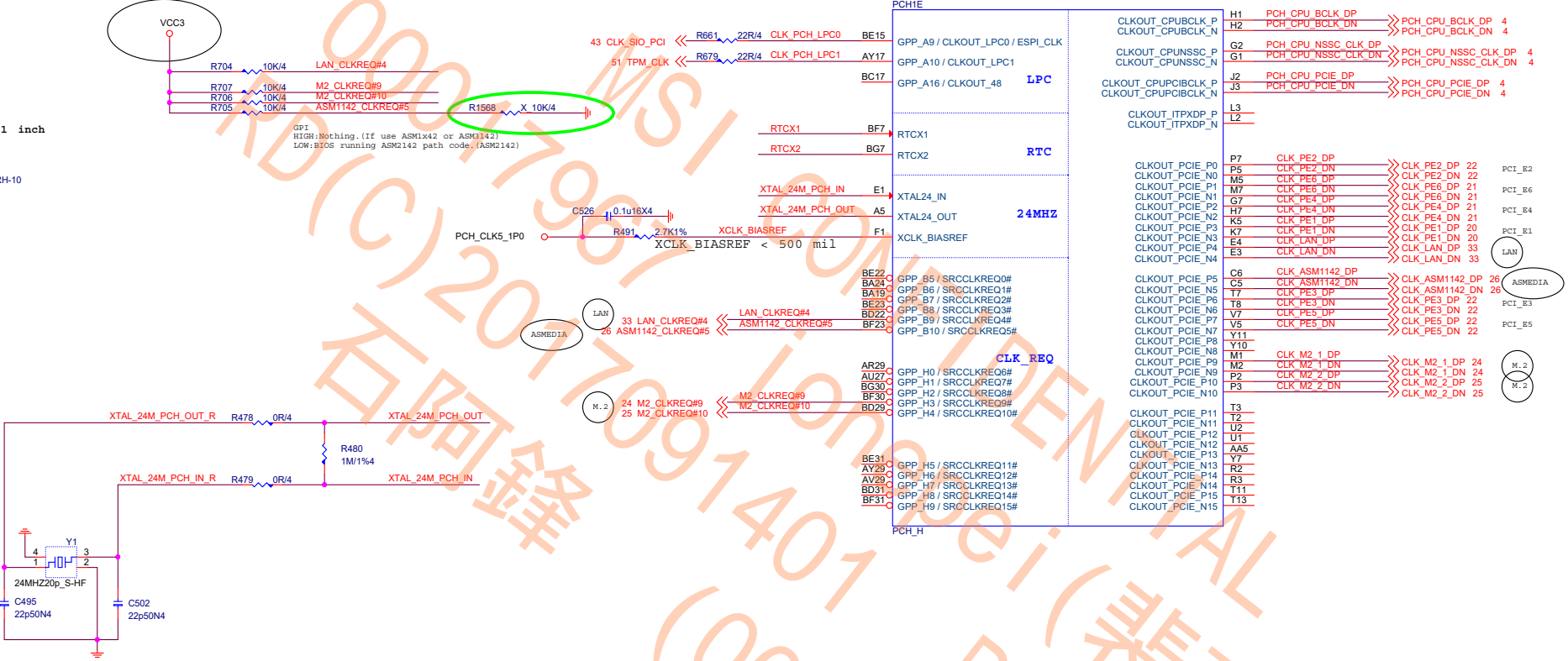
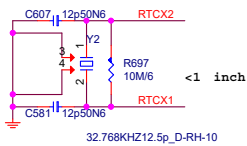




PCH_CLK

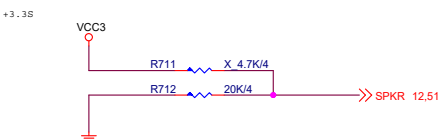
RTC Block

Close to PCH



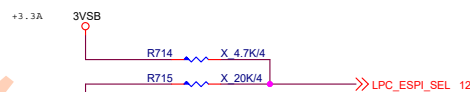


TOP Swap



Internal pull-down is disabled after PLTRST#

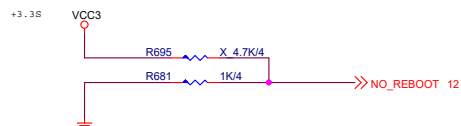
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

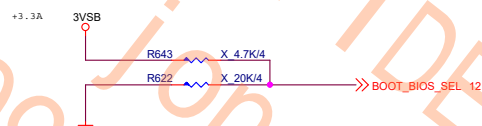
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

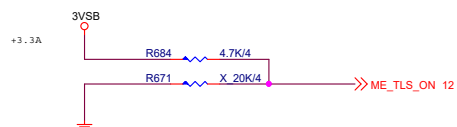
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

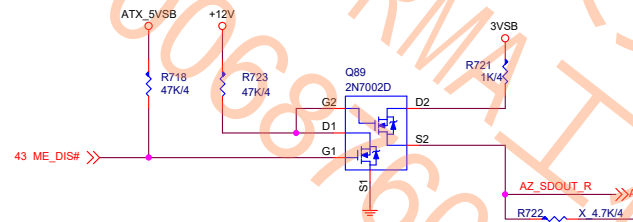
AMT and SBA with confidentiality



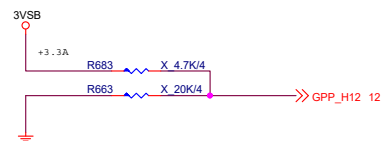
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

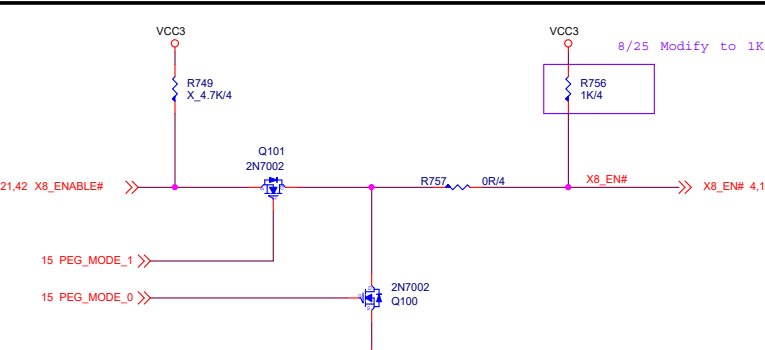
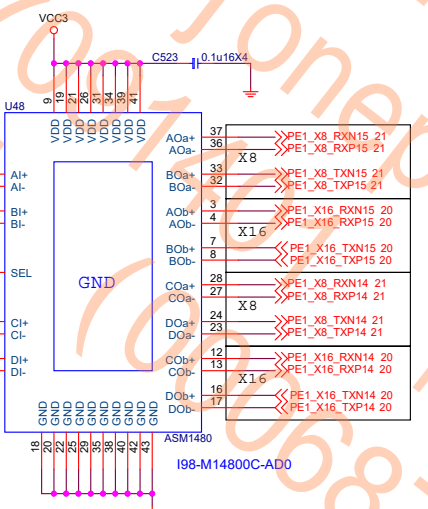
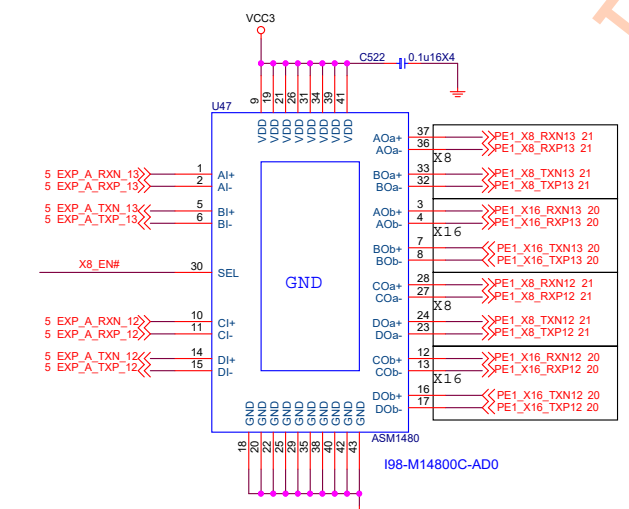
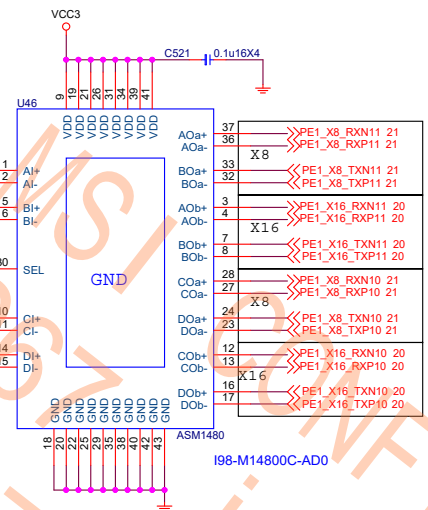
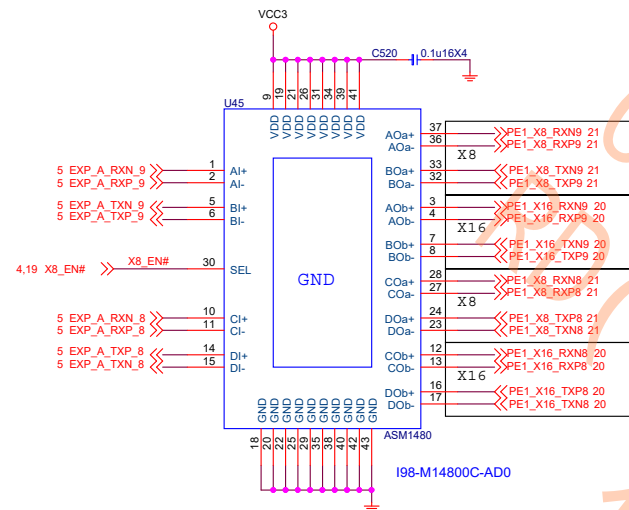
Internal pull-down is disabled after RSMRST



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MODE_1

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0	MODE_1
AUTO	0	1

If USE HW MODE
GPP_G0 & GPP_G1 programming to GPI

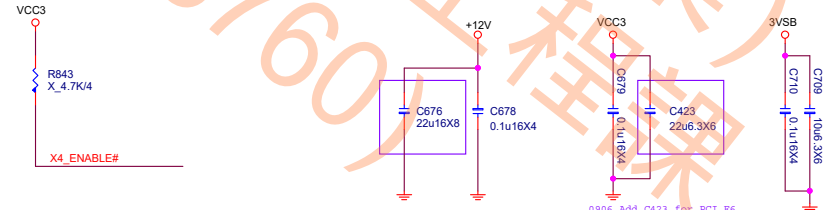
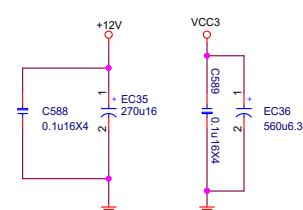
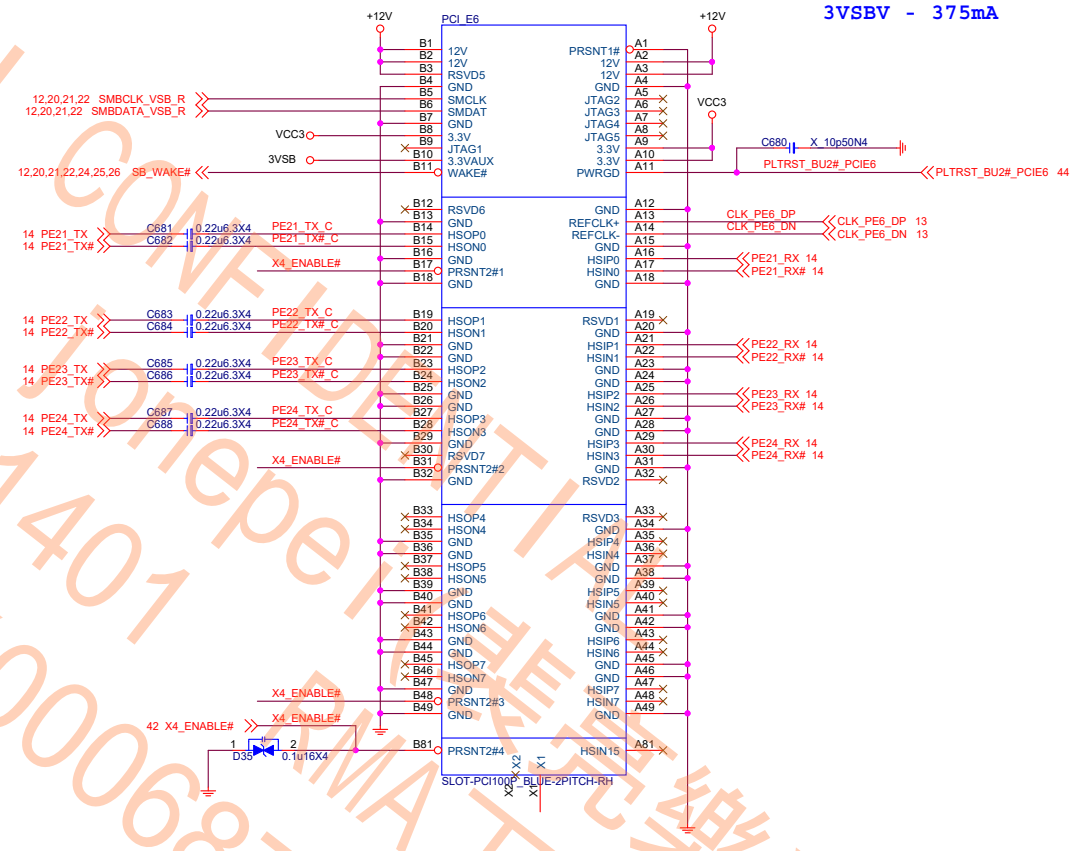
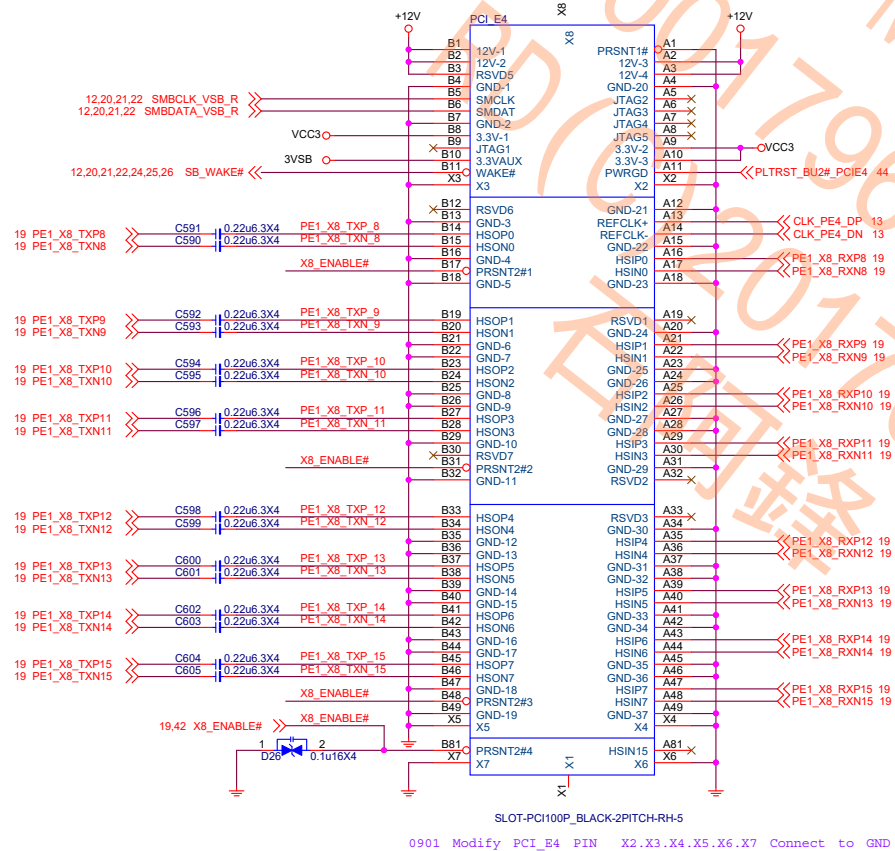
If USE BIOS MODE
GPP_G0 & GPP_G1 programming to GPO

BIOS MODE

PCH Status	MODE_0	MODE_1
16,0	0	0
8,8	1	0

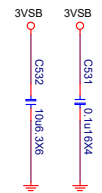
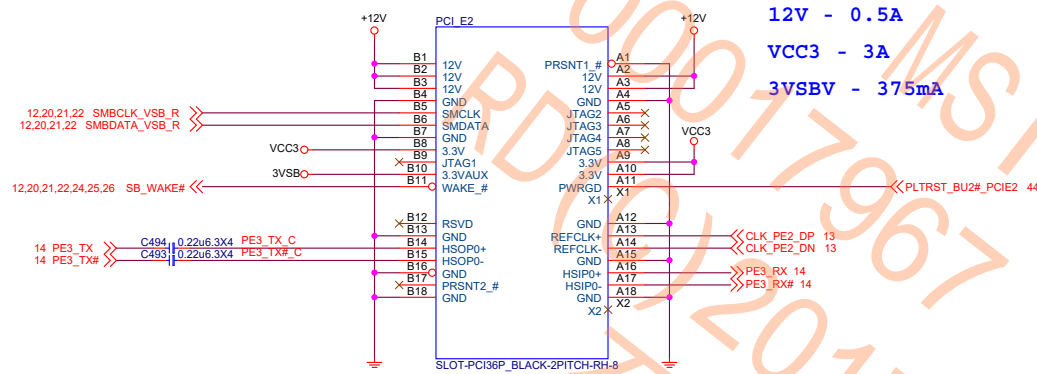
PCI Express X4 Slot

12V - 2.1A
VCC3 - 3A
3VSBV - 375mA

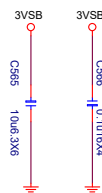
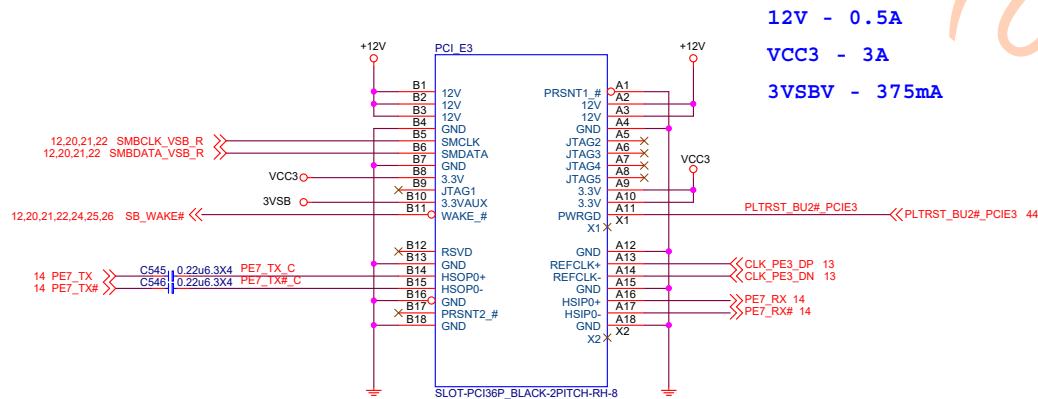


MICRO-STAR INT'L CO.,LTD				
MS-7B45				
Size	Document	Description		Rev
Custom		PCIE SLOT (X4)		20
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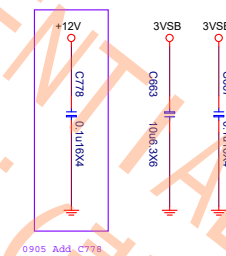
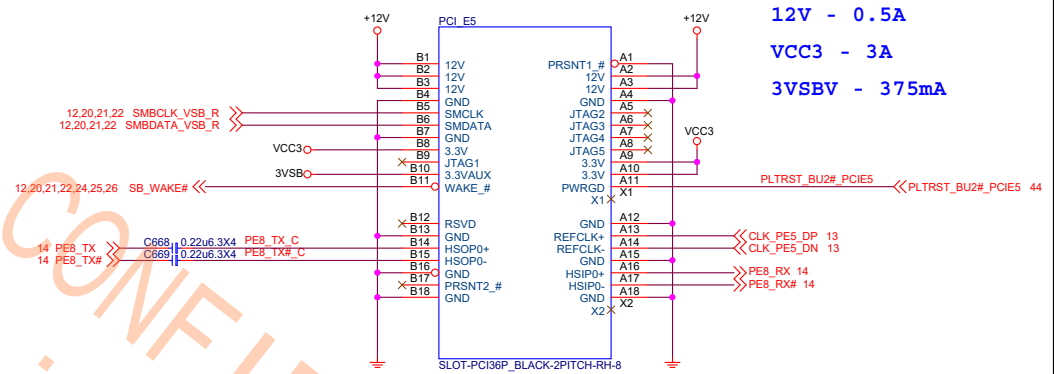
2016.08.25 Modify to N11-0360211-F02



2016.08.25 Modify to N11-0360211-F02



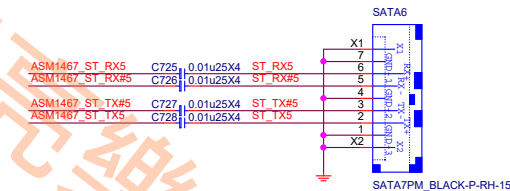
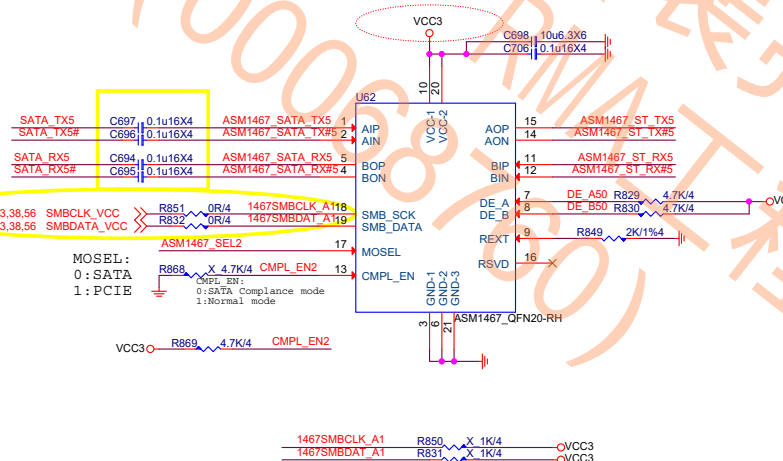
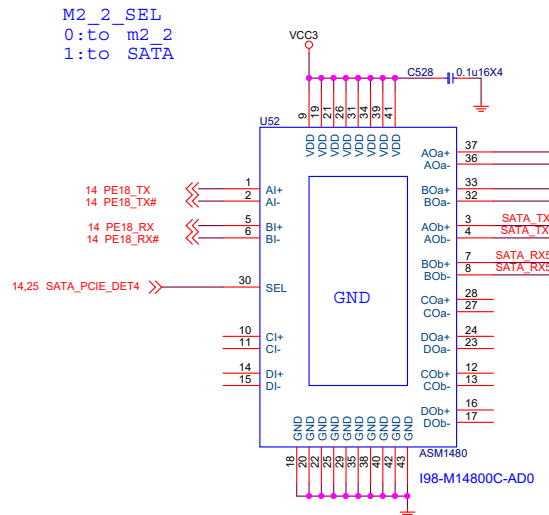
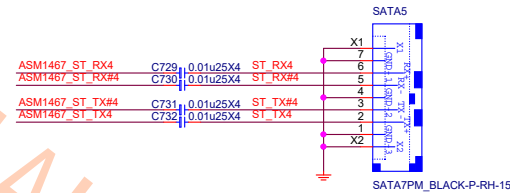
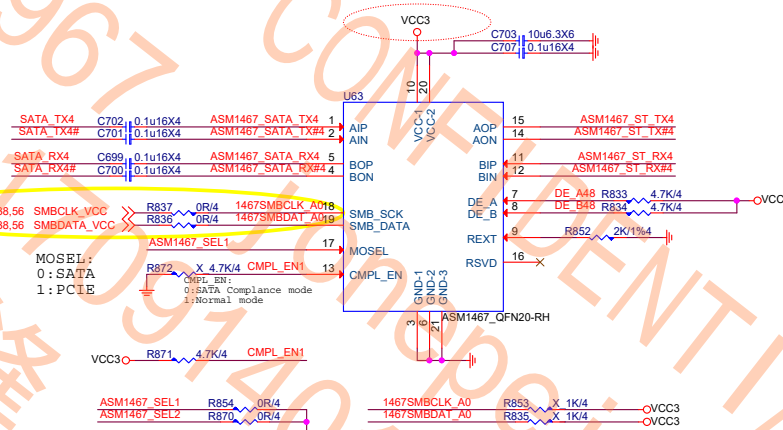
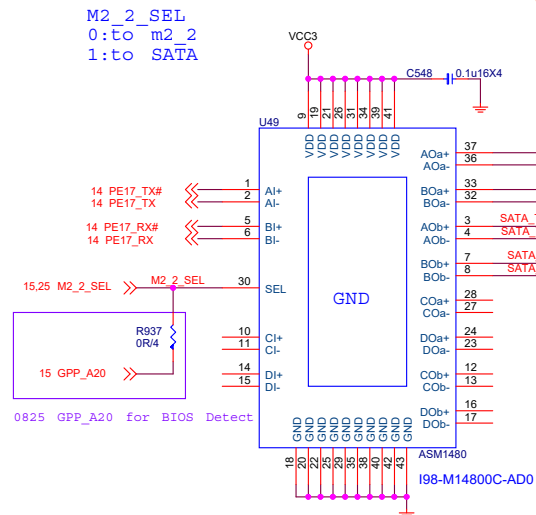
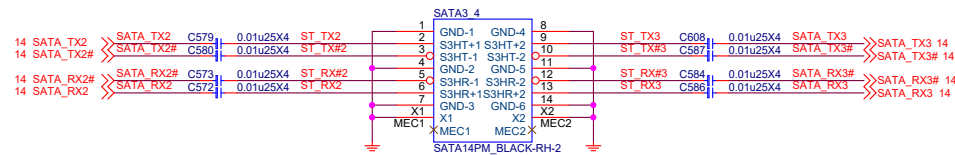
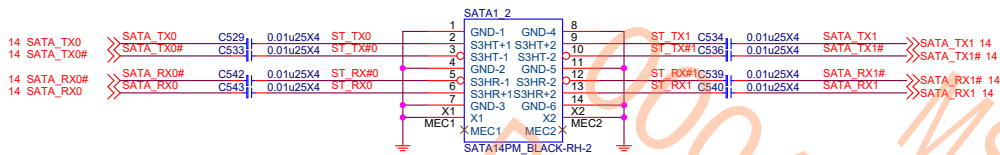
2016.08.25 Modify to N11-0360211-F02

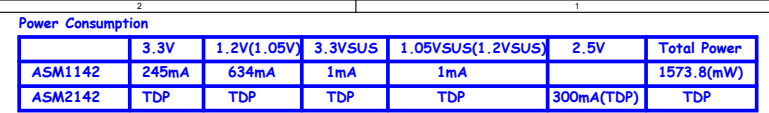


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```
1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2
```

ASM1142 1.2 VCC Power

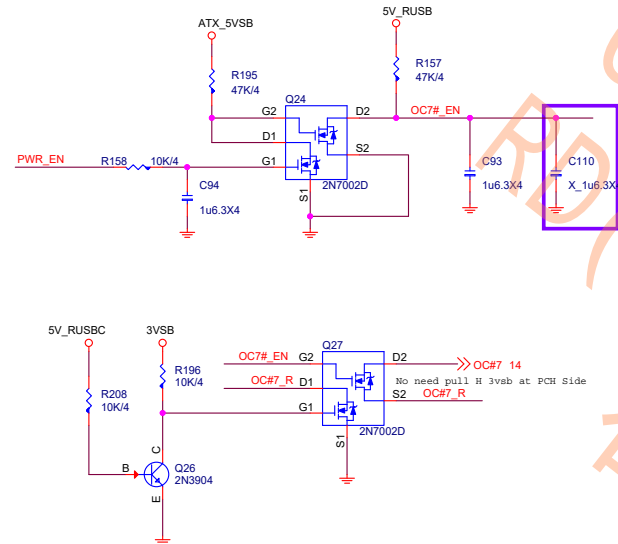
ASM1142 1.2 VSB Power

EEPROM

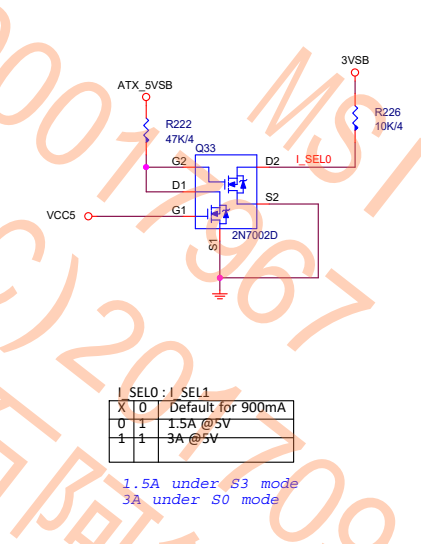


Size Custom	Document Description ASM 1142	Rev 20
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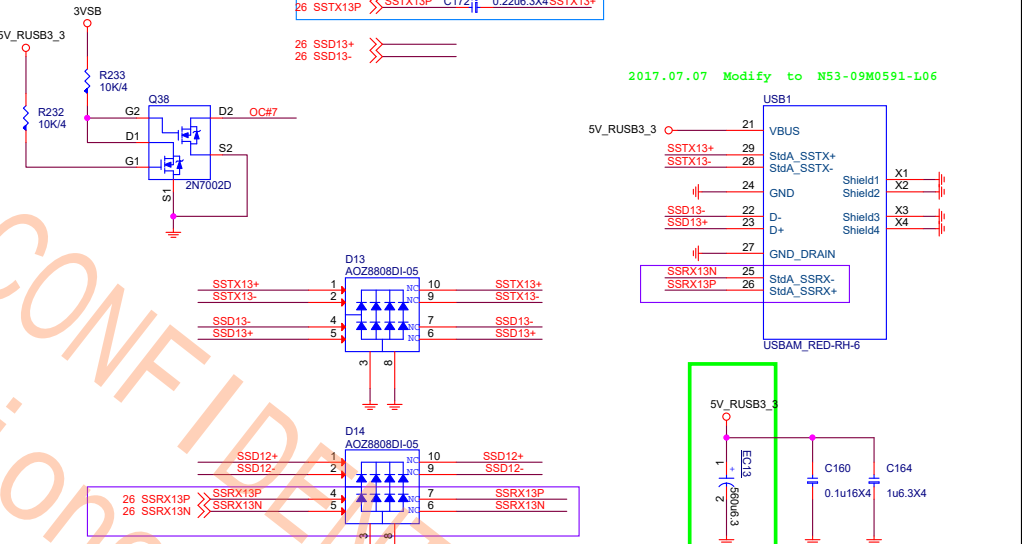
VBUS OC#



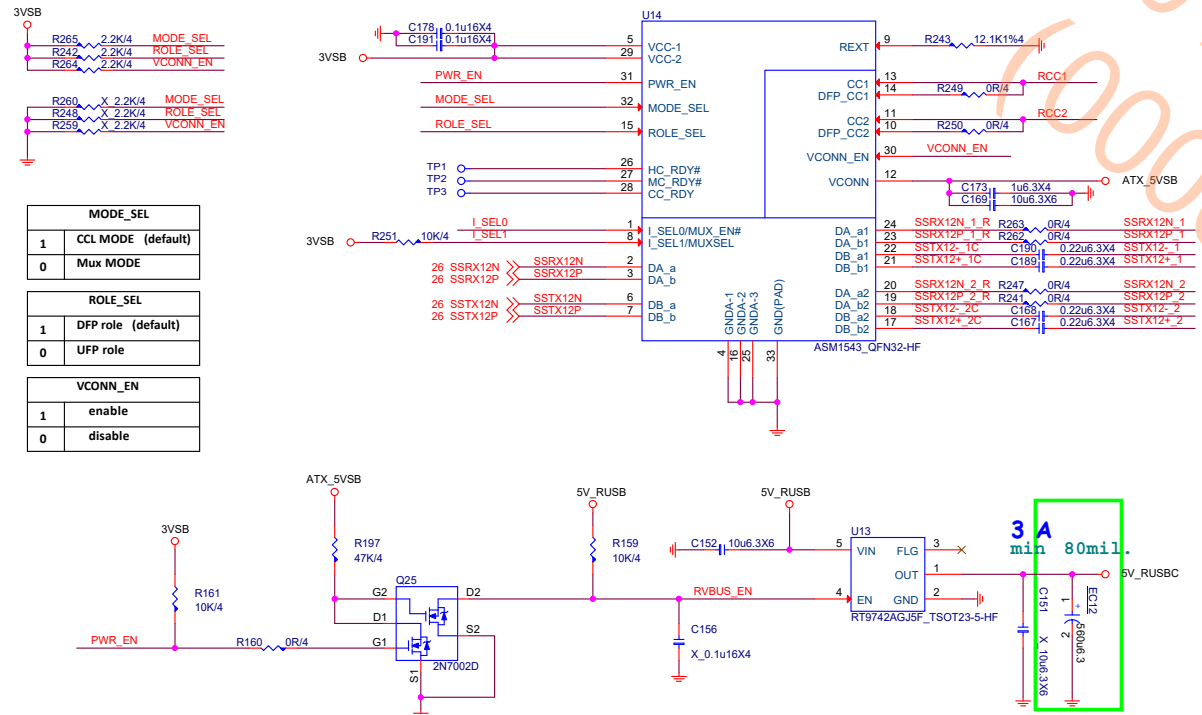
Current Mode



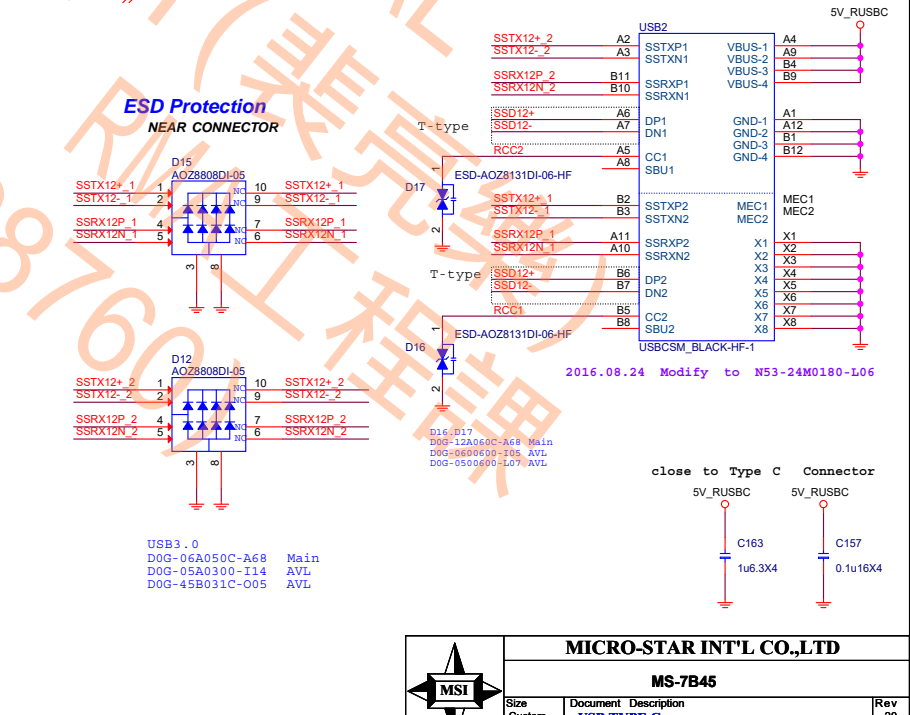
TYPE-A



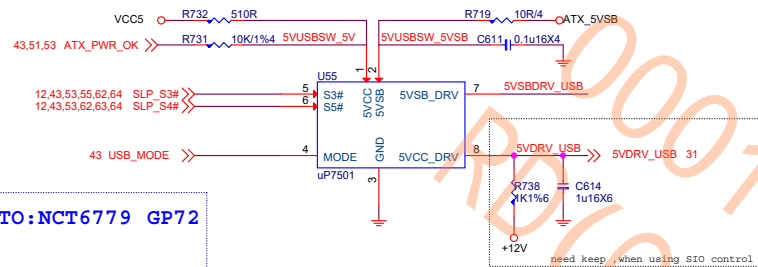
USB Type-C MUX with Configuration Channel (CC)



TYPE-C

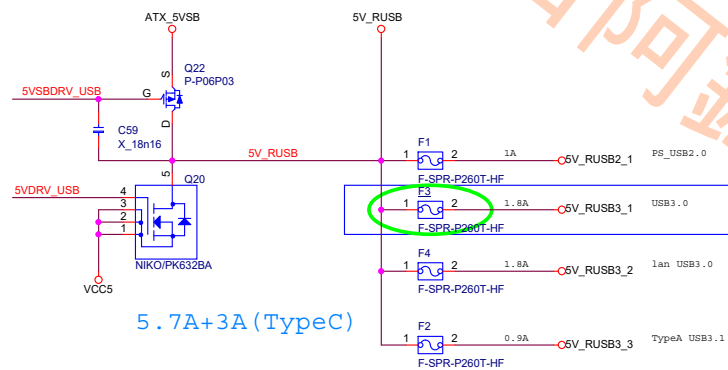


USB PORT POWER

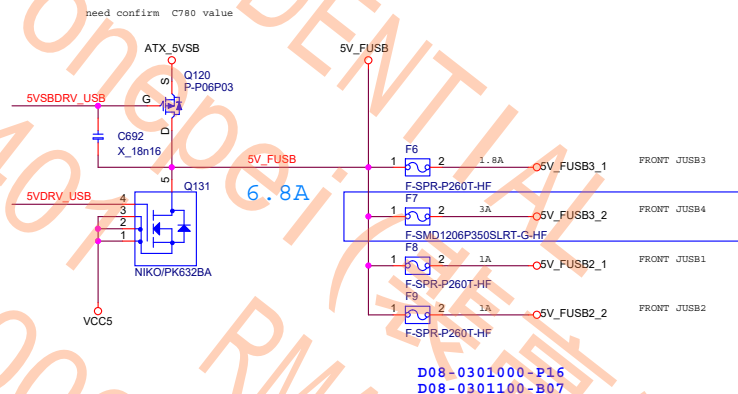


5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

REAR USB PORT POWER



FRONT USB PORT POWER



P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

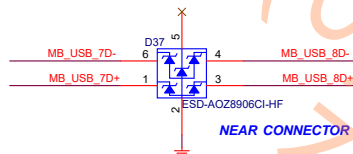
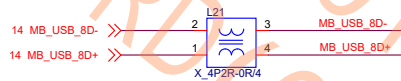
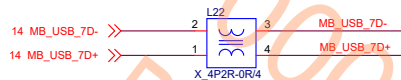
D08-0301000-P16
D08-0301100-B07



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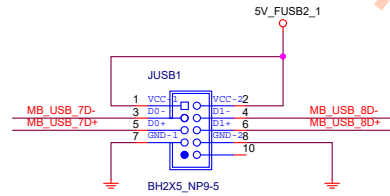
MS-7B45

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Custom		USB POWER UP7501	20
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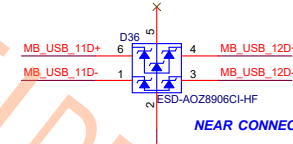
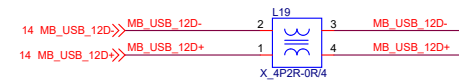
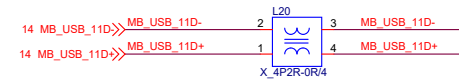
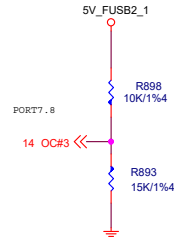
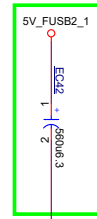
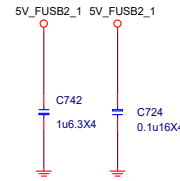


Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

1.0A

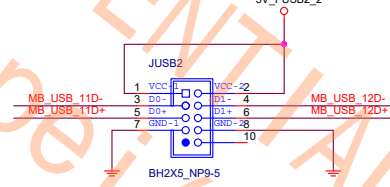


EMI Cap near Connector.

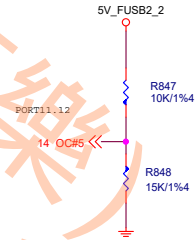
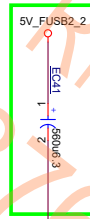
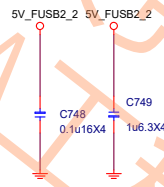


Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

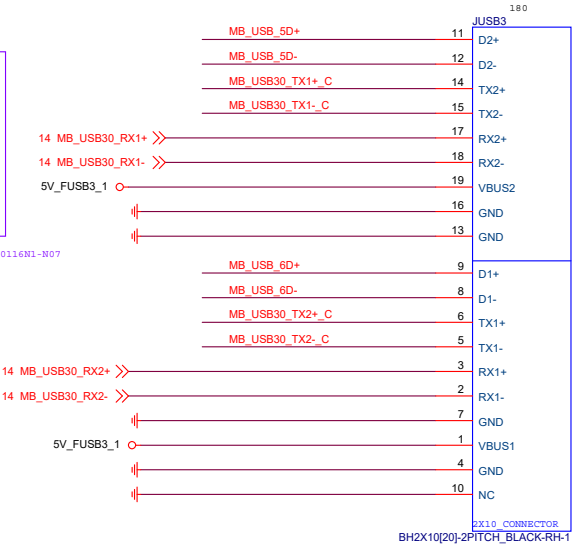
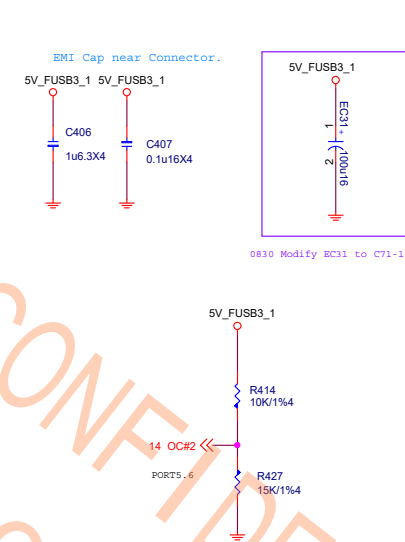
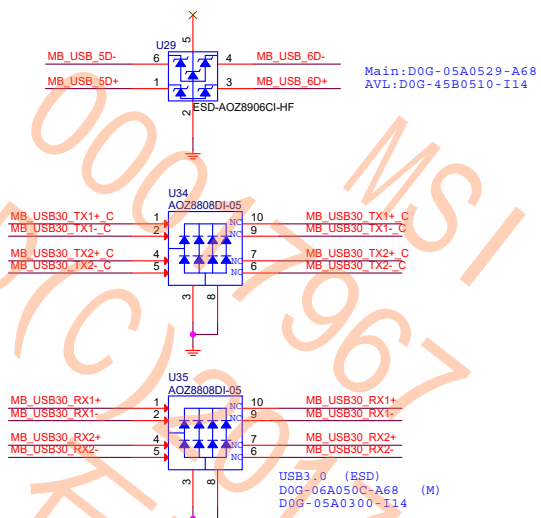
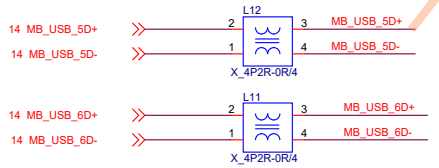
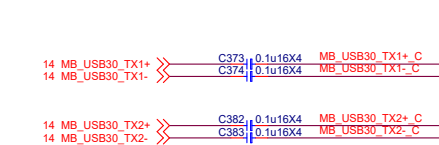
1.0A



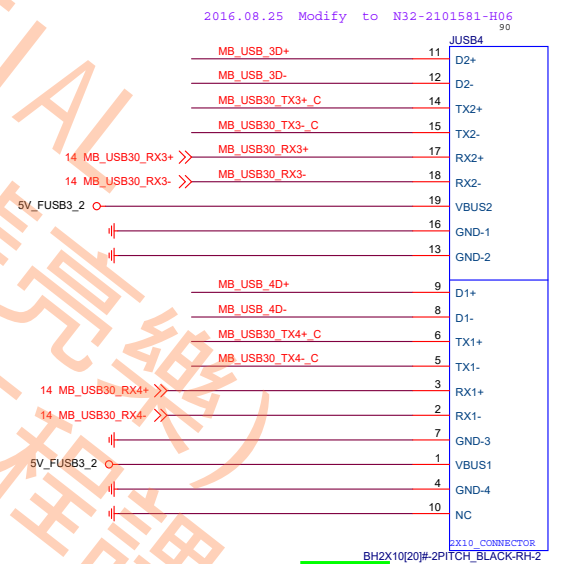
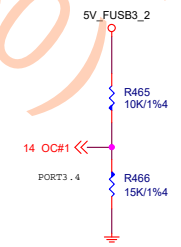
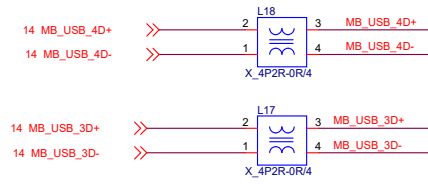
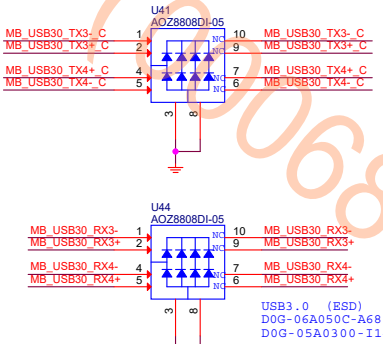
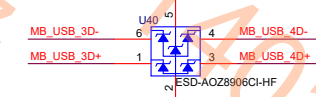
EMI Cap near Connector.



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Custom		Front USB20	20
Date: Wednesday, July 12, 2017		Sheet 29 of 70	



2016.08.25 Modify to N32-2101091-H06



2016.08.25 Modify to N32-2101581-H06

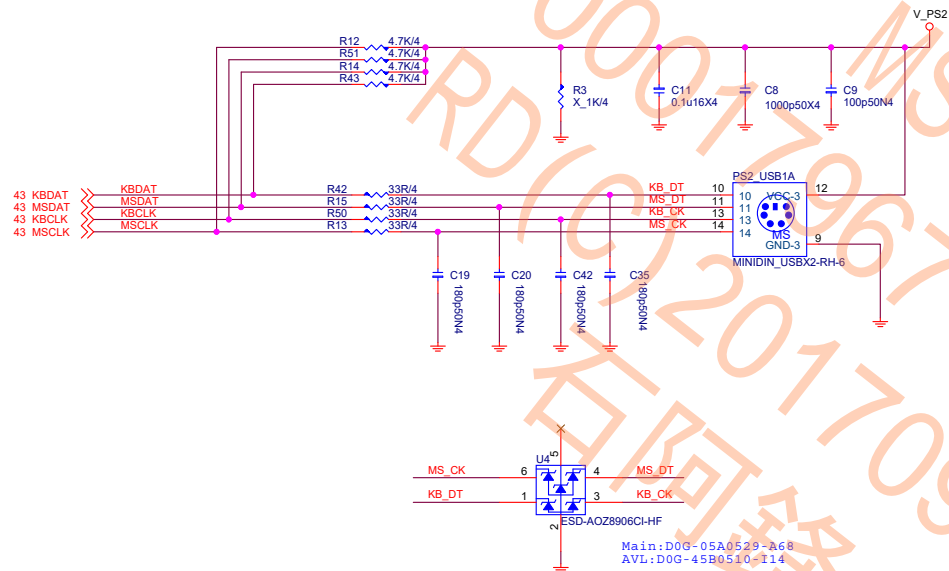
MSI

MICRO-STAR INT'L CO.,LTD

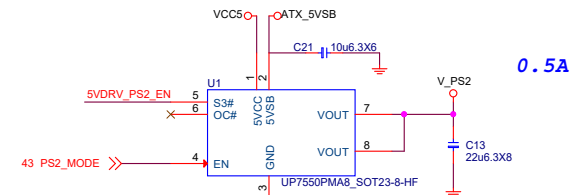
MS-7B45

Size	Document	Description	Rev
Custom		Front USB30	20
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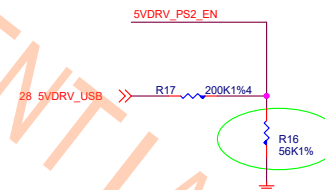
PS2 Connector



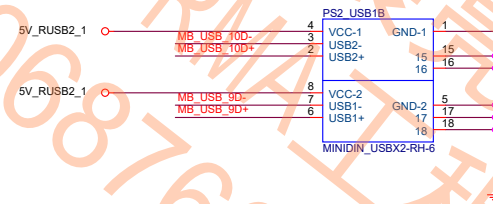
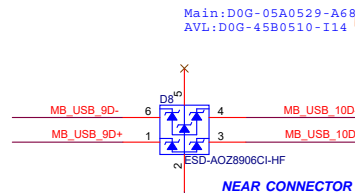
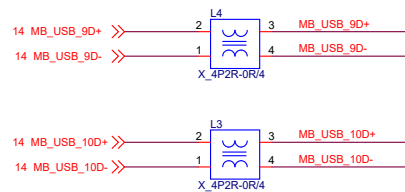
PS2 Power



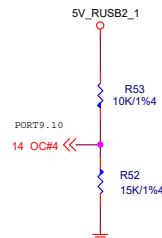
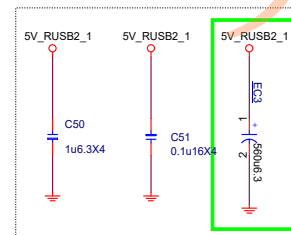
USB MODE



PS2 _USB



Close to Connector

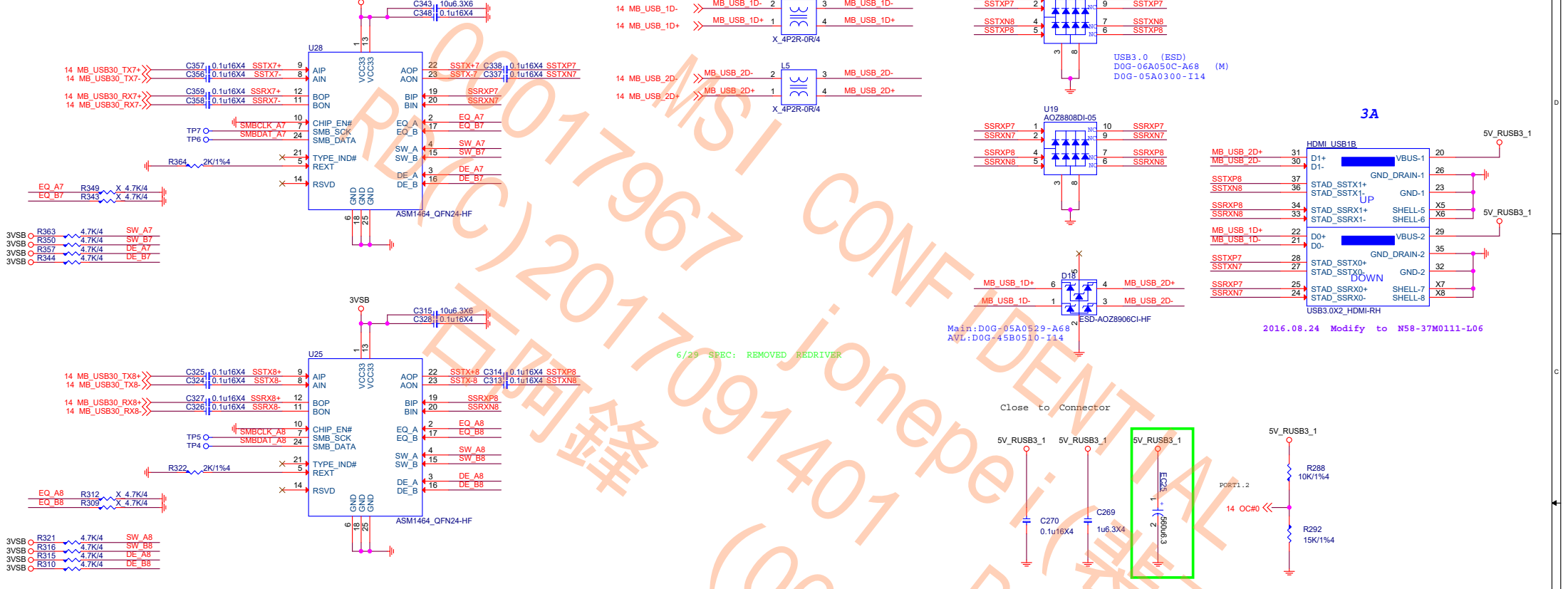


MICRO-STAR INT'L CO.,LTD

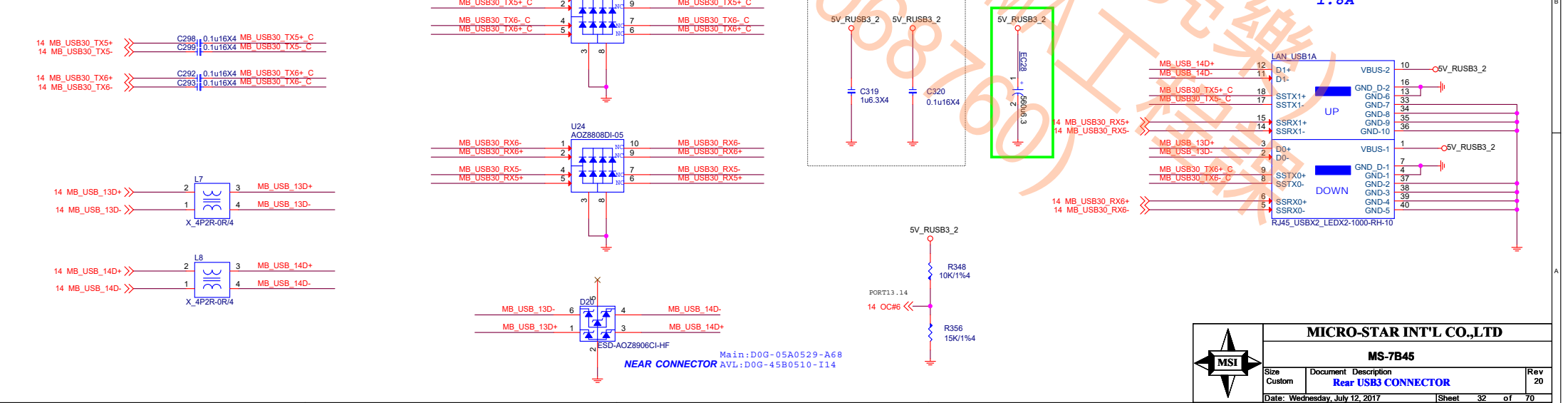
MS-7B45

Size	Document	Description	Rev
Custom		Real USB2&PS2 CONNECTOR	20
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HDMI USB3.0

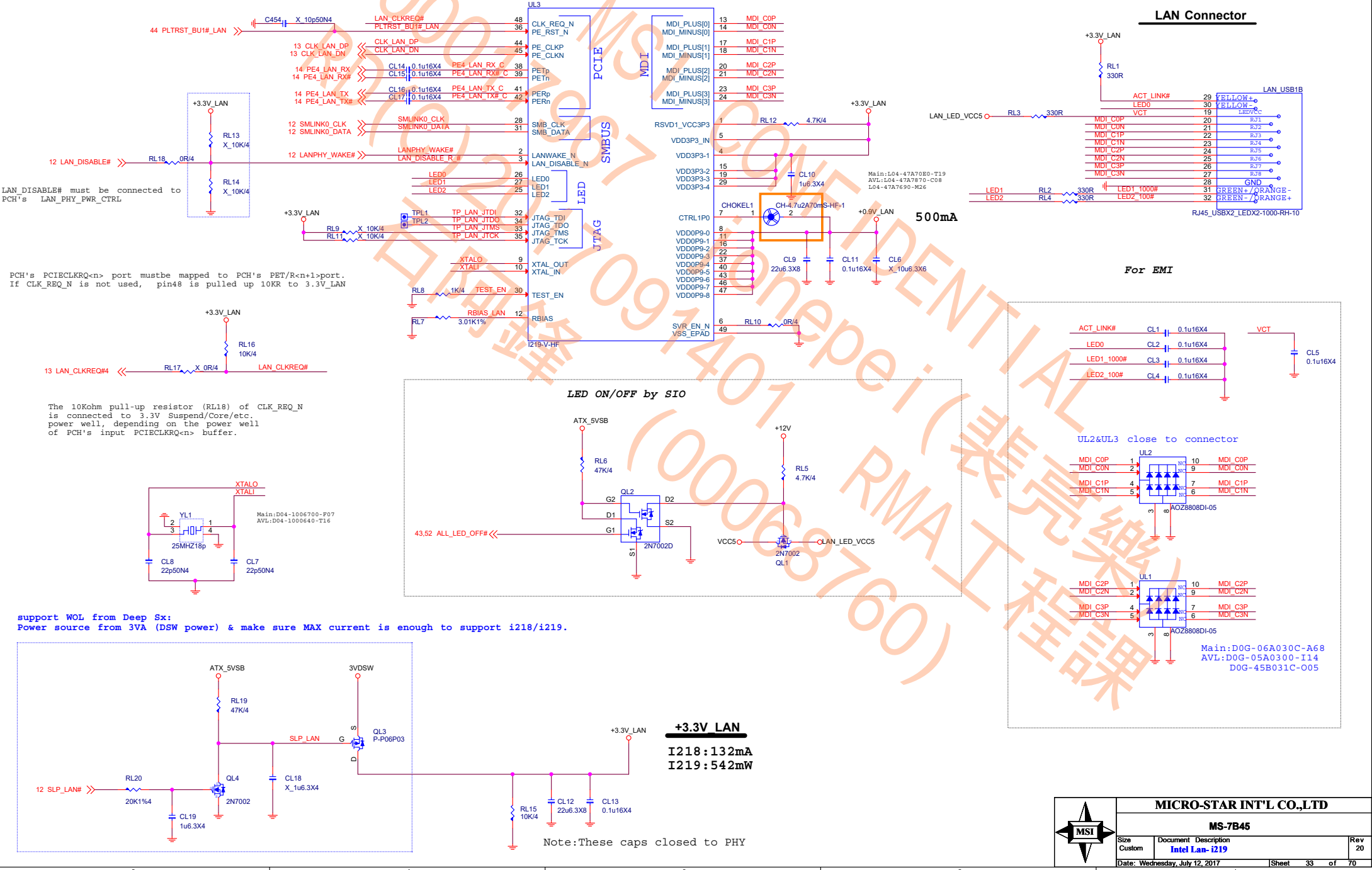


LAN USB3.0



Intel Lan- i219

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

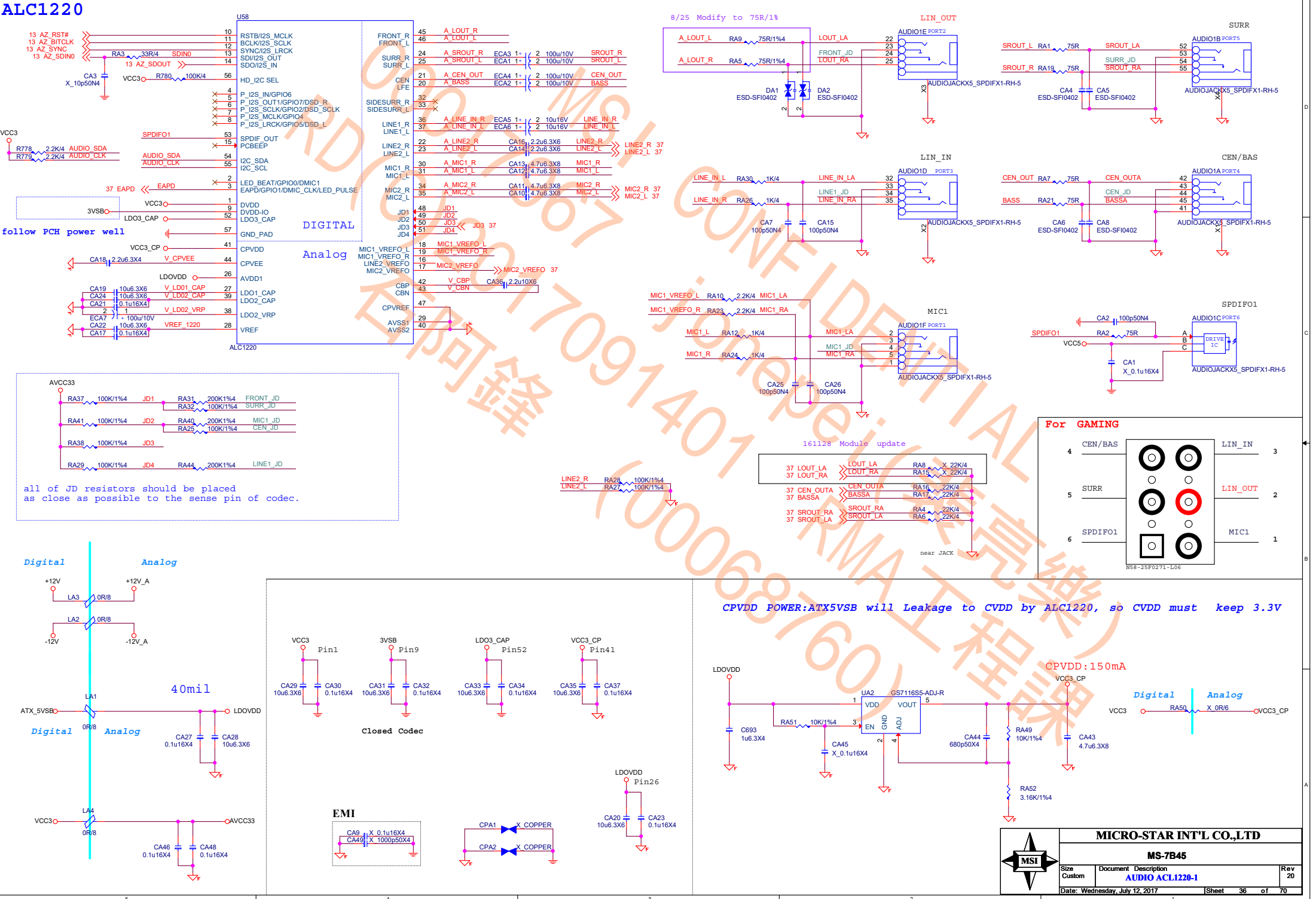


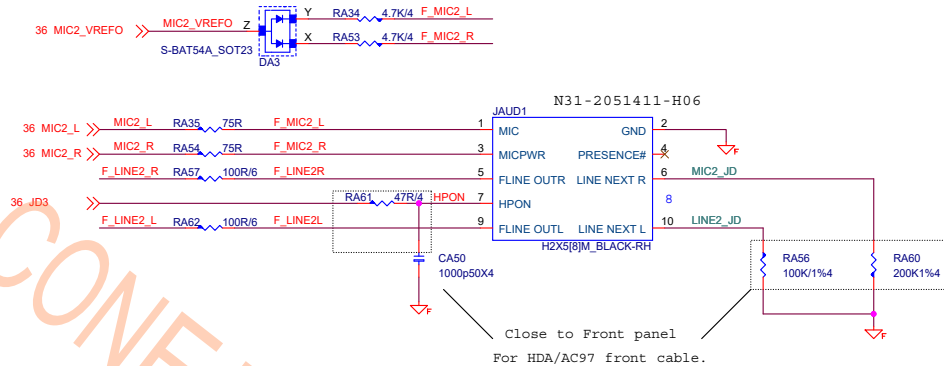
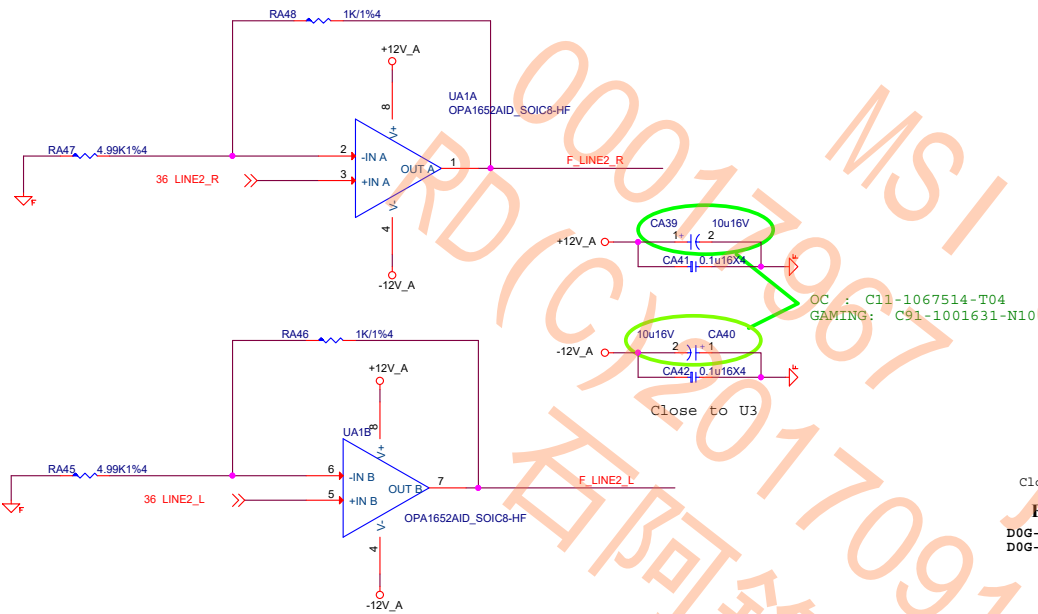
The schematic shows the DP_VCCB trace starting from VCC3, passing through resistors R1539 (0R/8) and R1538 (0R/8), and then connecting to pin 3 (VCCB) of the U105 chip. The trace also passes through a capacitor C1375 (10u6 3X6). Other connections include TP65 and TP66 to SCL A and SCL B pins, and various control signals like SDAA, SCL A, SCL B, and SCL C. Power pins are connected to VCC5 and EN. Signal pins include P_AUX_DP+, P_AUX_DP-, C_AUX_DP+, and C_AUX_DP-. The U105 chip is identified as NCT3532Y-OFN16-HF.



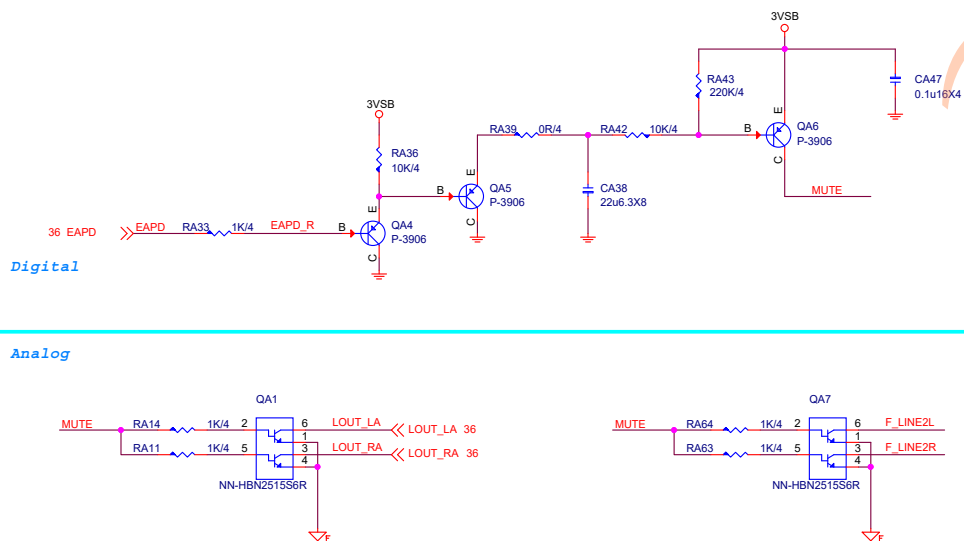
MS-7B45

ALC1220

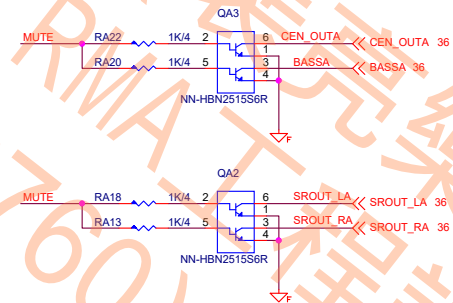




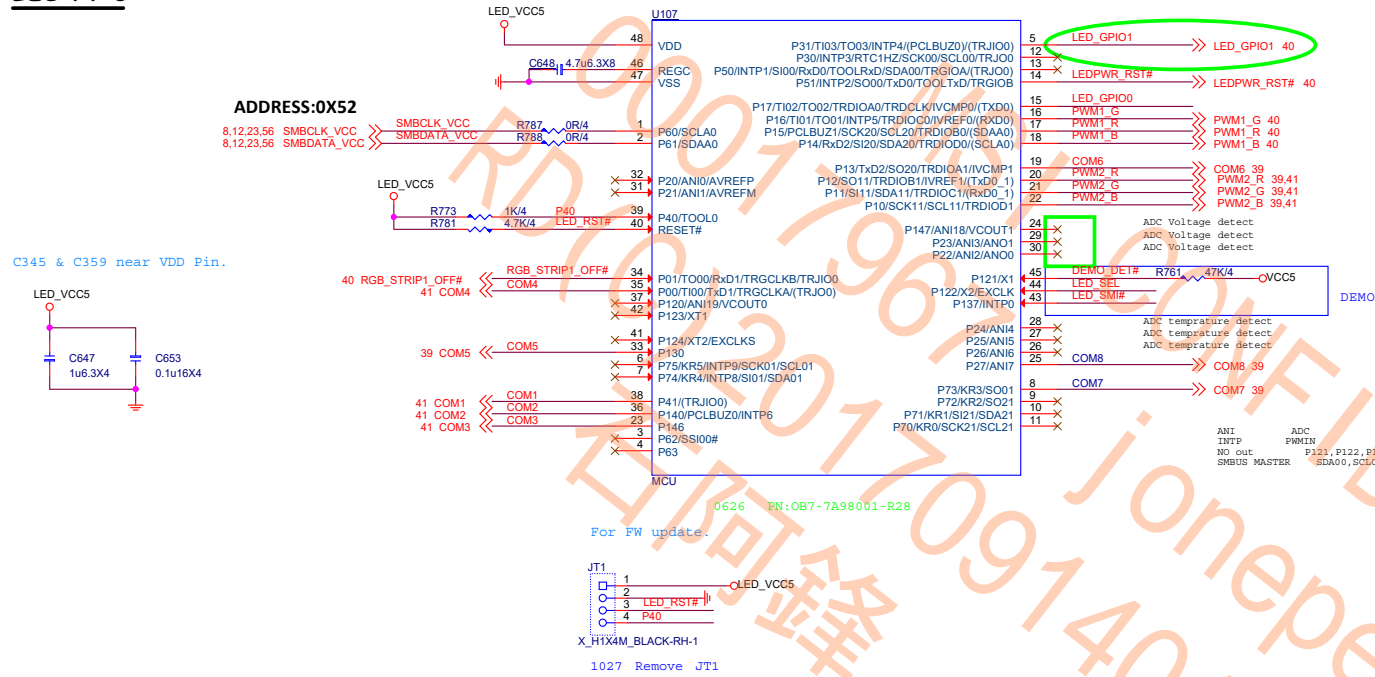
Rear Line OUT De-POP circuit
(De-pop circuit for Rear Line out & Front Headphone out)



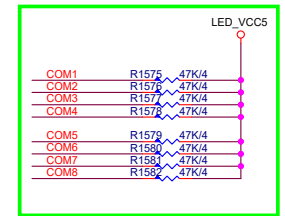
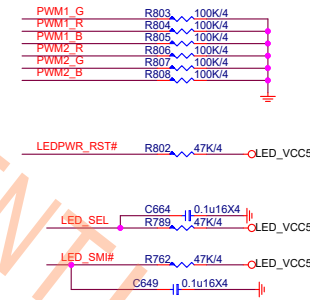
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA4, CA5, CA6, to TVS)



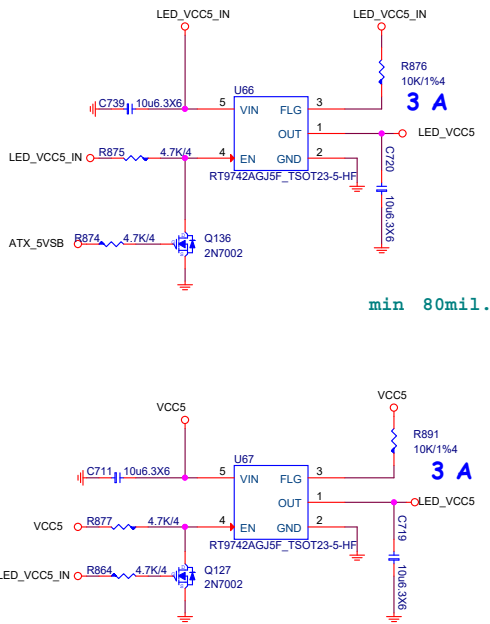
LED MCU



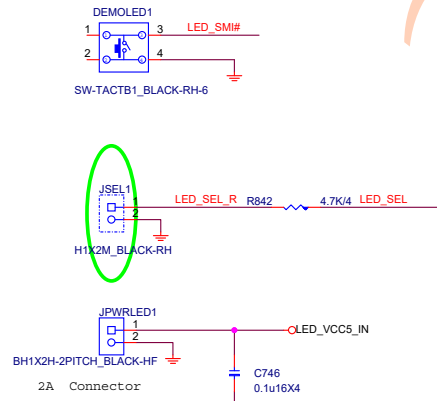
Control	Net Name	PWM USE	Connector
PCH	LED_GPIO1	No Use	JPIPE_LED2
Audio	COM1-4	PWM2	RGB LED
Board Side LED	COM5-8	PWM2	RGB LED
LED STRIPLINE	RGB_STRIP1_OFF#	PWM1	JLED1
LED STRIPLINE	RGB_STRIP1_OFF#	PWM1	JLED2
IO Cover	LED_GPIO0	No Use	JPIPE_LED1



EXTERNAL POWER INPUT

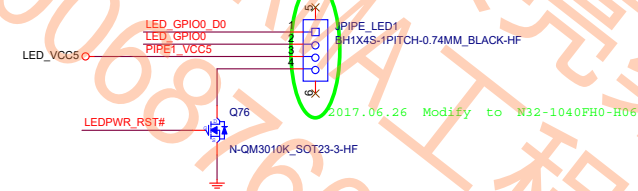


LED Demo Button



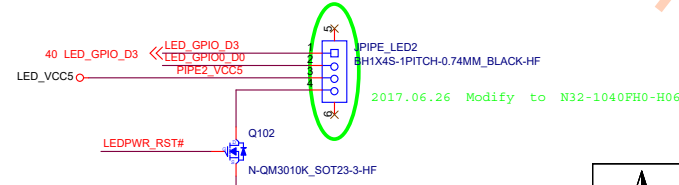
Cover LED

6PCS LED*0.16W=0.96W



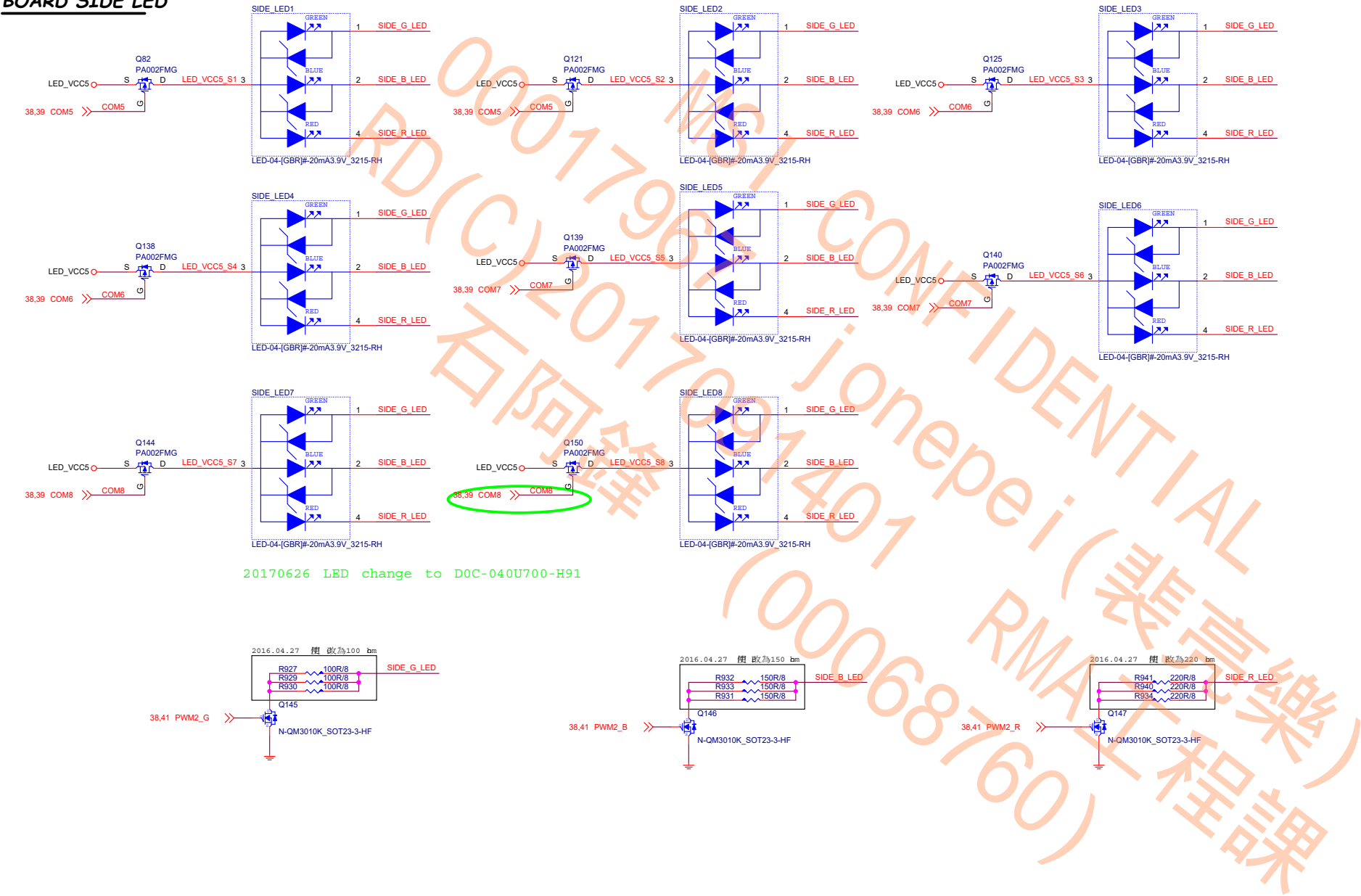
HEATSINK LED

9PCS LED*0.16W=1.44W

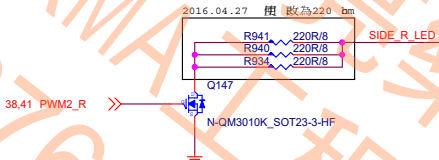
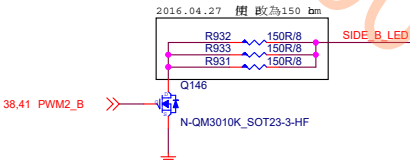
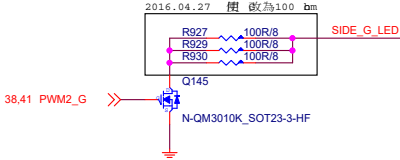


MICRO-STAR INT'L CO.,LTD			
MS-7B45			
Size	Document	Description	Rev
Custom		LED MCU Control	20
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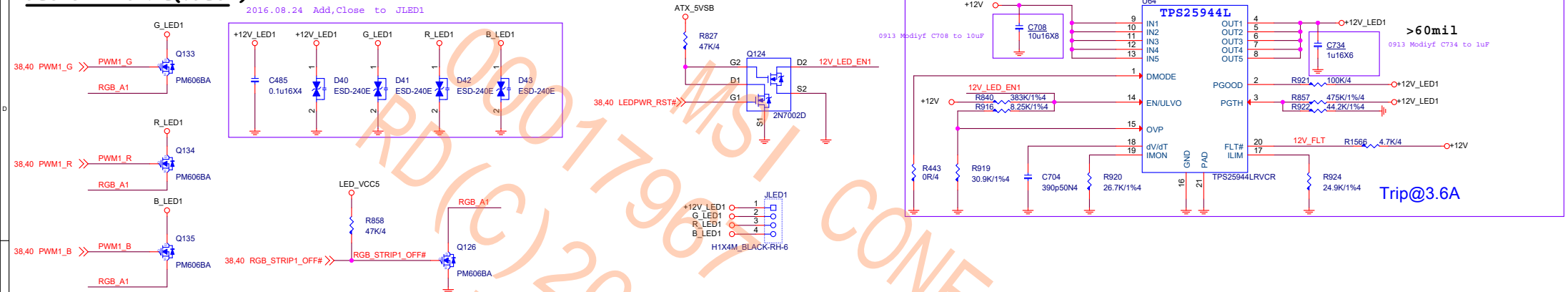
BOARD SIDE LED



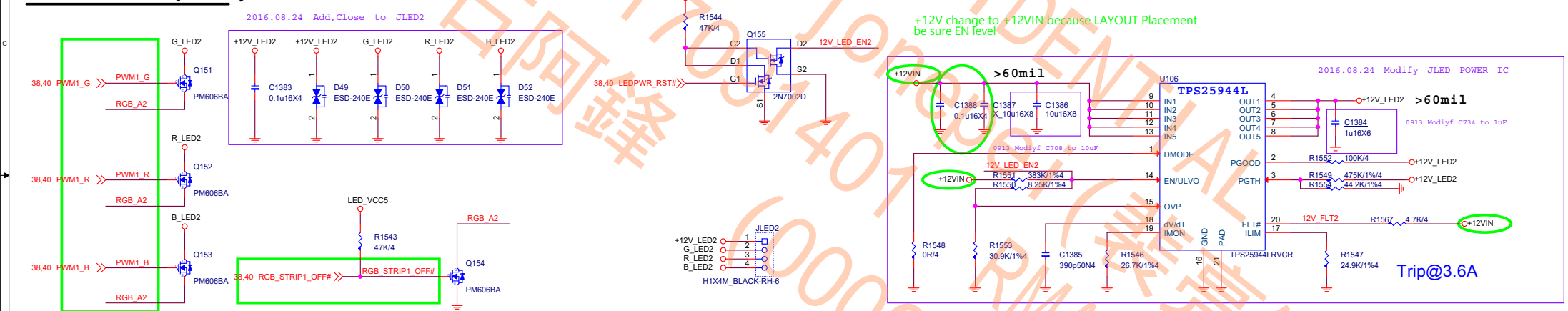
20170626 LED change to D0C-040U700-H91



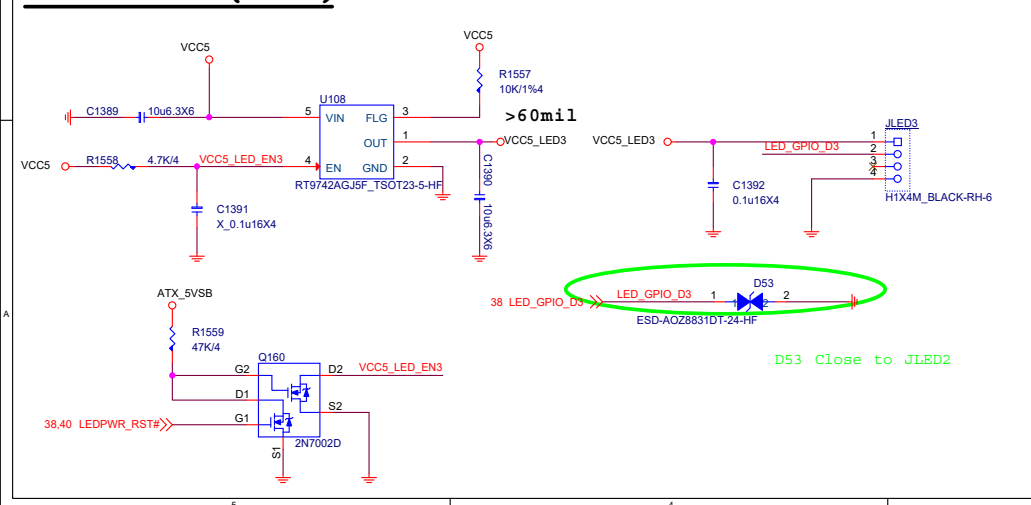
LED STRIPLINE(JLED1)



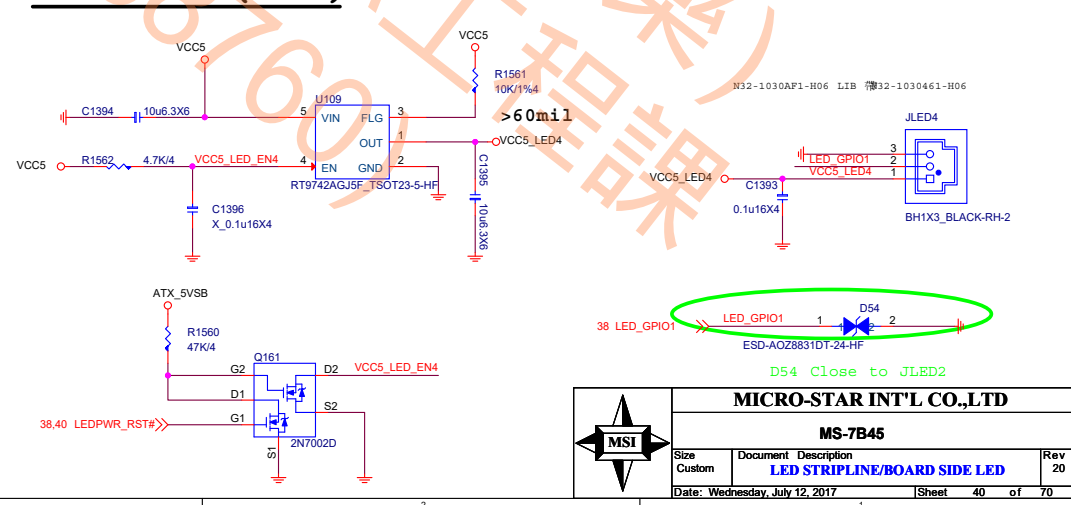
LED STRIPLINE(JLED2)



LED STRIPLINE(JLED3)



LED STRIPLINE(JLED4)

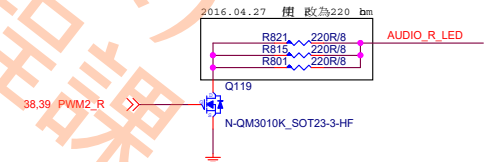
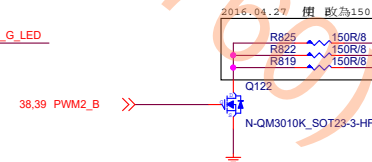
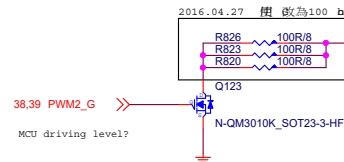
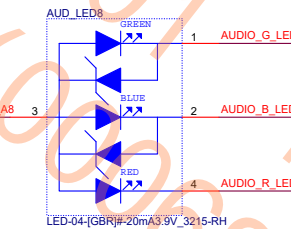
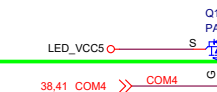
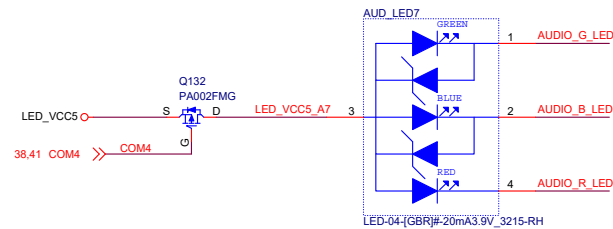
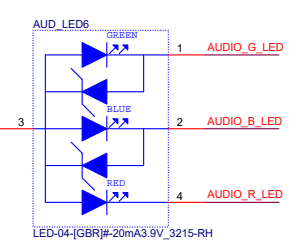
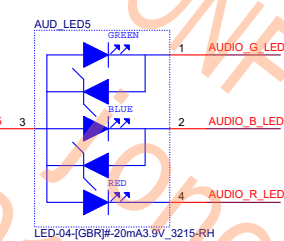
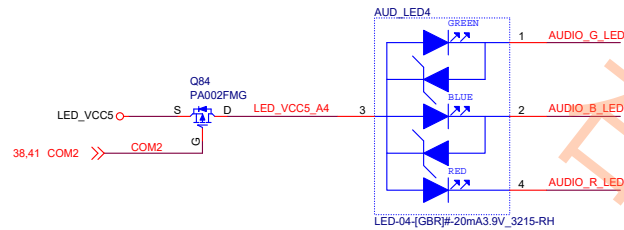
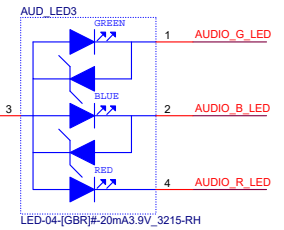
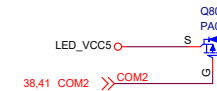
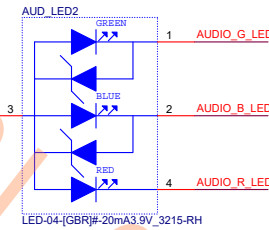
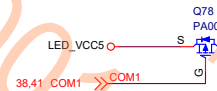
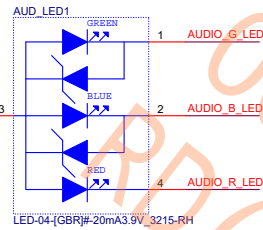


MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description LED STRIPLINE/BOARD SIDE LED	Rev 20
Date: Wednesday, July 12, 2017		Sheet 40 of 70

20170626 LED change to D0C-040U700-H91



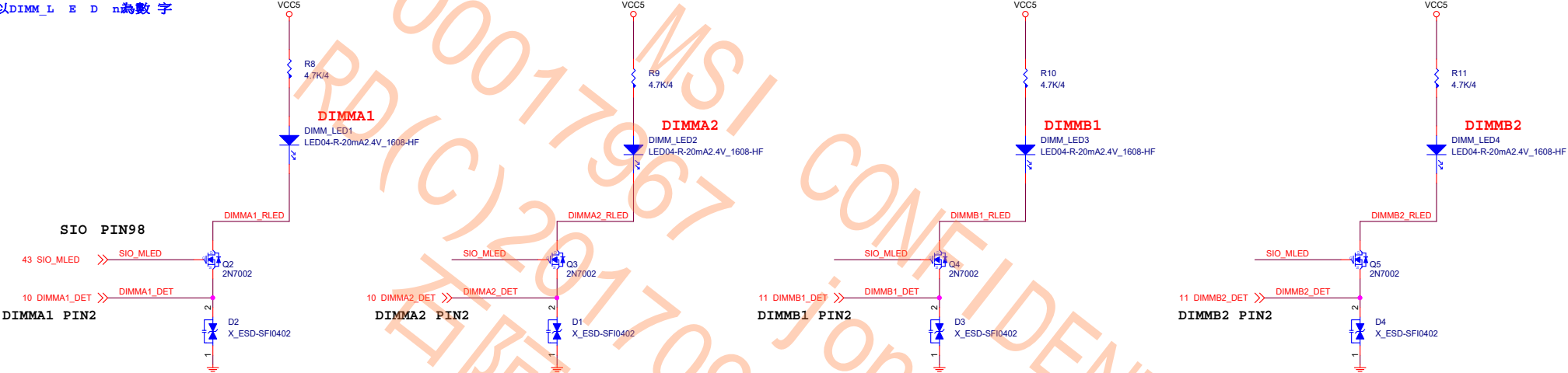
MS-7B45

Size Custom	Document Description LED AUDIO	Rev 20
Date: Wednesday, July 12, 2017		Sheet 41 of 70

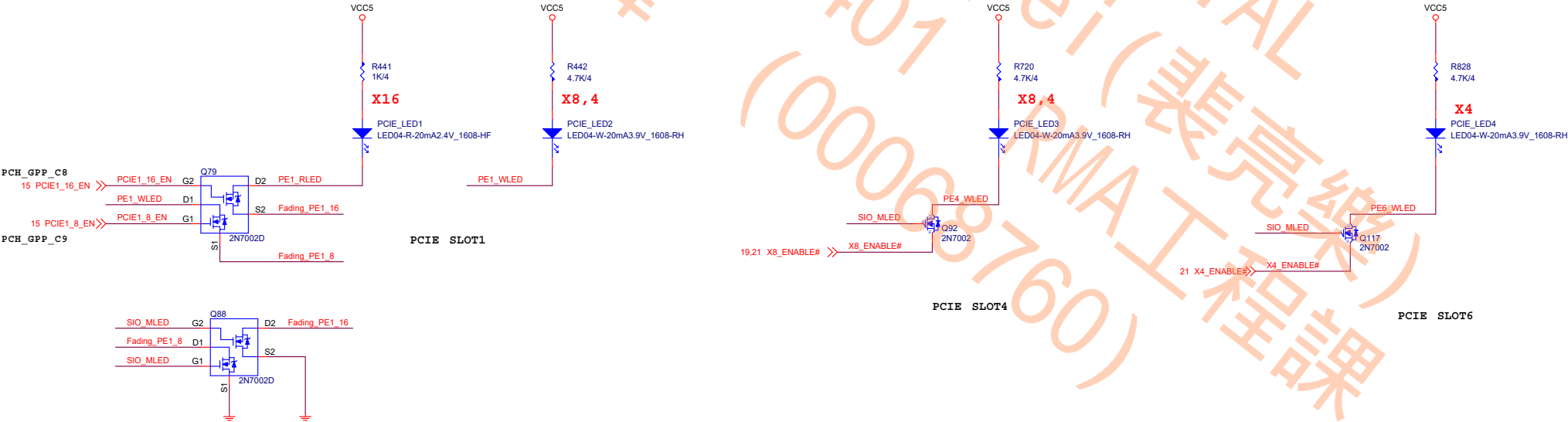
DIMM_SLOT

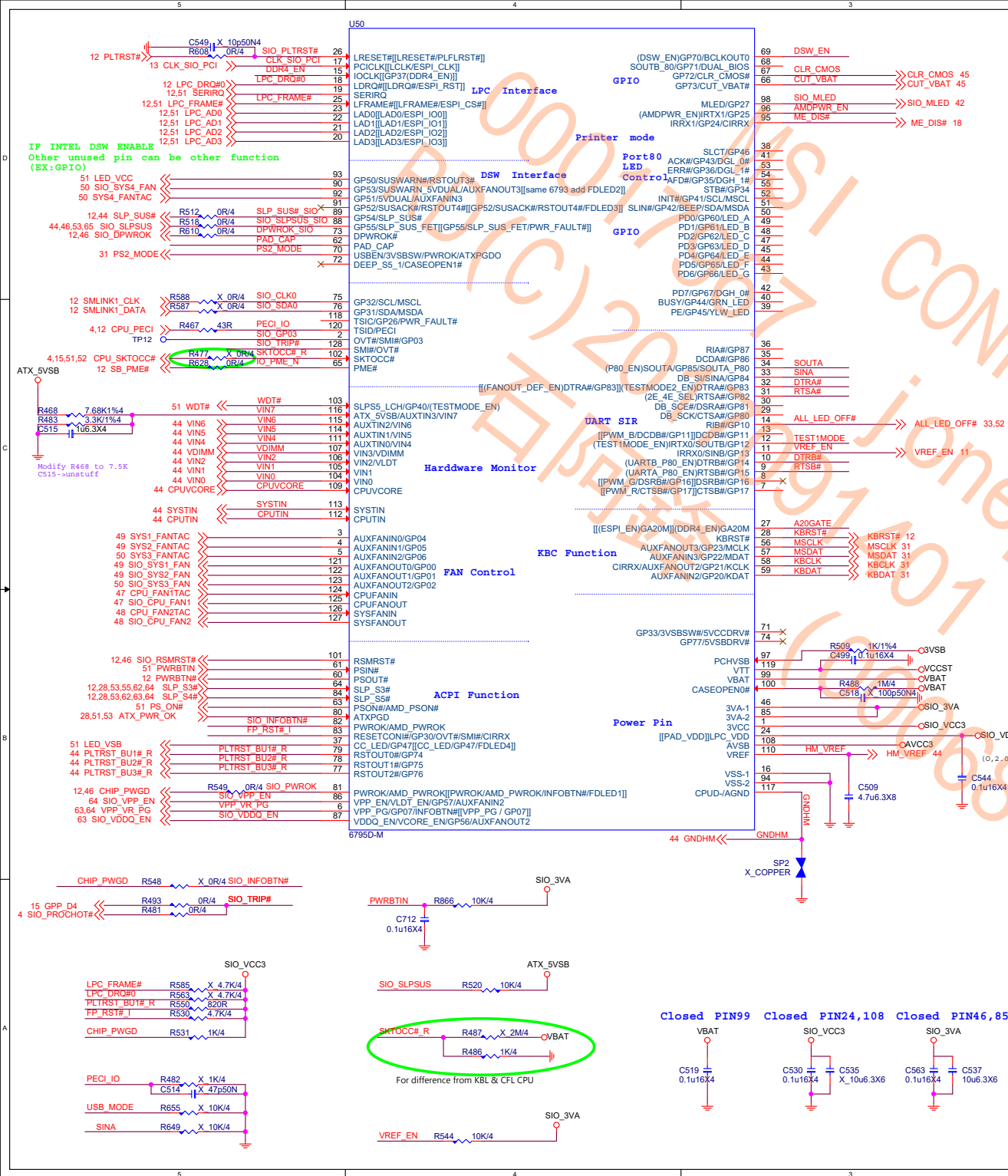
紅： D0C-040S500-E07

LED 繼以DIMM_L E D n為數字



PCIE_SLOT LED





POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795	NAME	Circuit	NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	RTSB#	DISABLE	ENABLE	UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DTRB#	DISABLE	ENABLE	UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	TEST1MODE	DISABLE	ENABLE	TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable		
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE		6793 Disable 6795 Disable	6793 Enable 6795 Enable		
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E			LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#		6793 disable 6795 default 50%	6793 Enable 6795 default 100%		INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80			LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW			INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ			INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE			INTERNAL RSMRST

Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO

3V Analog Power

Strapping Pin Details

Intel
6793 pull down
6795 pull down

6793 DDR4_EN strapping
6795 ESPI_EN strapping

6793 pull high
6795 LPC pull down/ESPI pull high

MICRO-STAR INT'L CO.,LTD

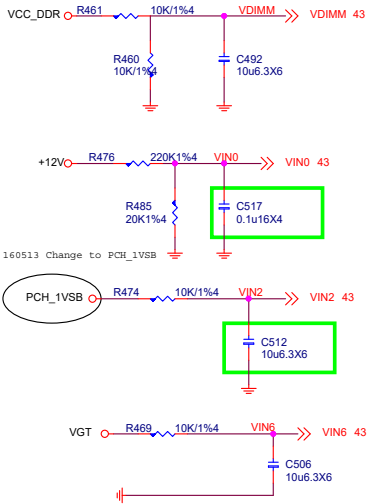
MS-7B45

Size	Document	Description	Rev
Custom		SIO-NTC6792D-1	20

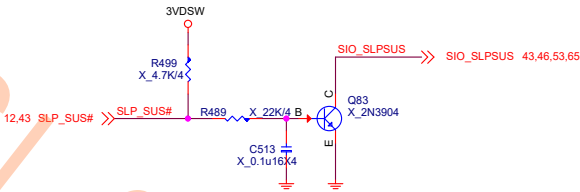
Date: Wednesday, July 12, 2017 | Sheet 43 of 70

HW Monitor - Voltage

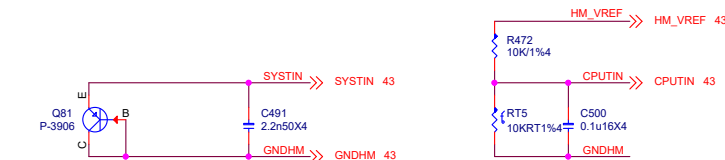
SIO HM Voltage voer 2V will not detect



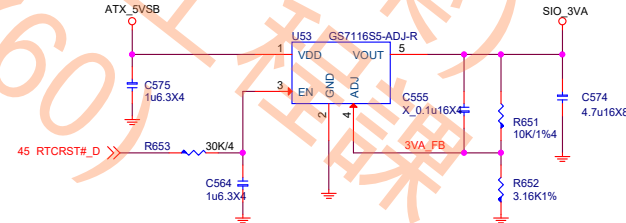
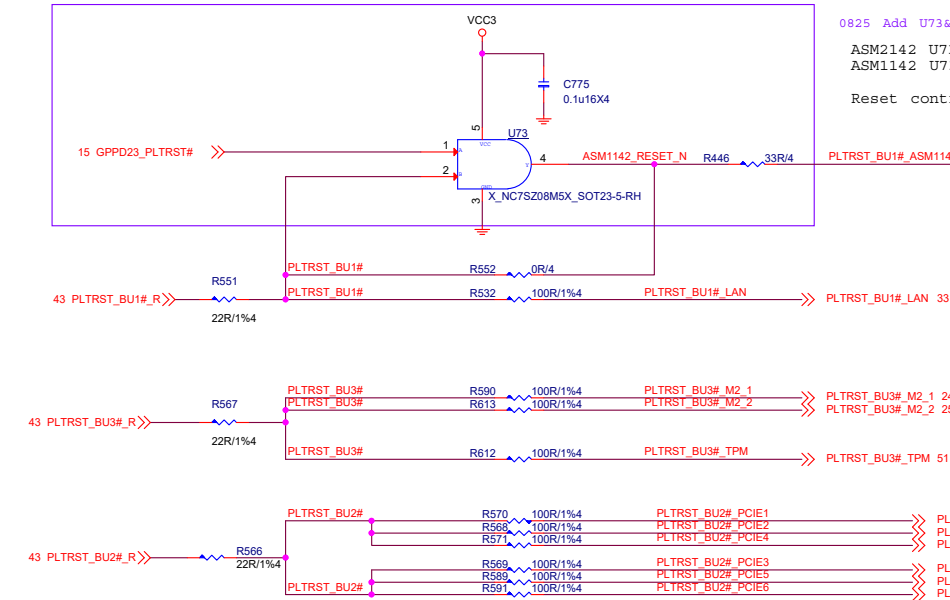
SLP_SUS Co-lay circuit



Thermal Monitor



0825 Add U73&R446 for ASM2142 PLTRST#
ASM2142 U73 stuff R552 unstuff
ASM1142 U73 unstuff R552 stuff
Reset control for ASM2142 only.



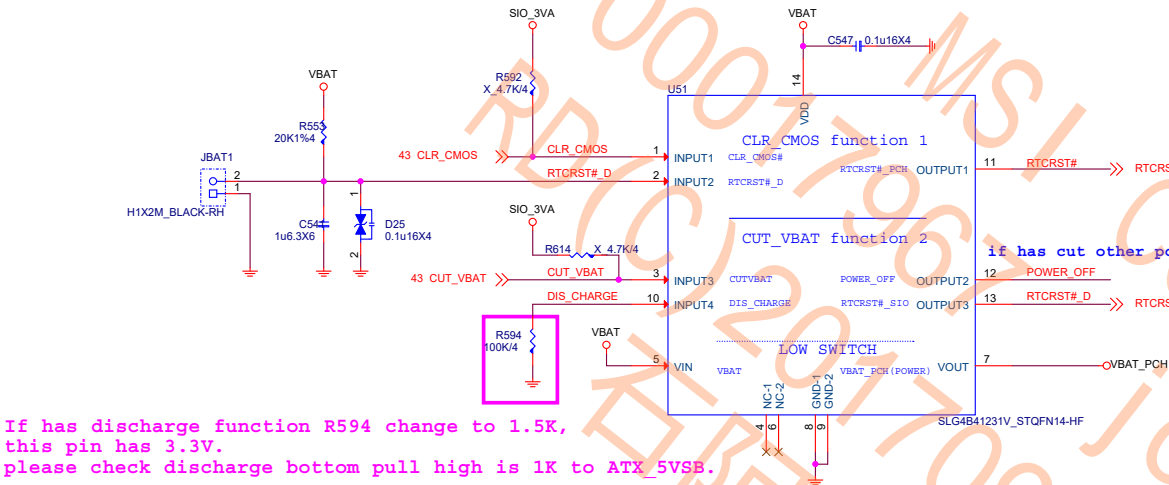
MICRO-STAR INT'L CO.,LTD

MS-7B45

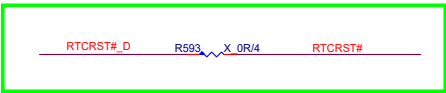
Size	Document	Description	Rev
Custom		SIO-NTC6792D-2	20
Date: Wednesday, July 12, 2017			Sheet 44 of 70

CLR_CMOS

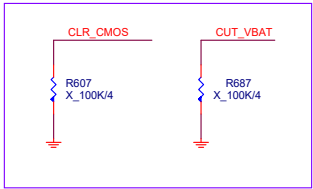
VBAT



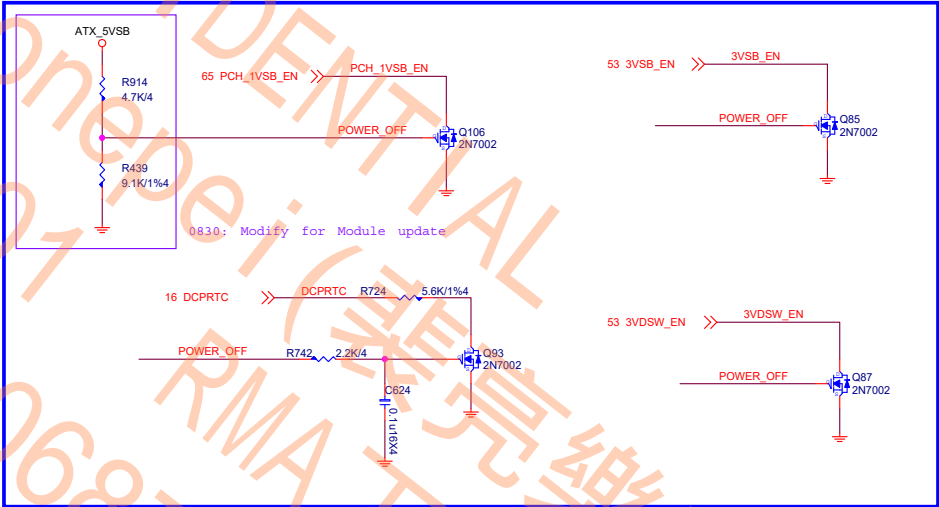
If has discharge function R594 change to 1.5K, this pin has 3.3V. please check discharge bottom pull high is 1K to ATX_5VSB.



Co-Lay NOT USE U12 , R139 STUFF
If STUFF R139 Please Check RTCRST# Double Pull High



0830: Add R607.R687 for Module update



Function 2					
IN		OUT			
INPUT3 & lowswitch EN		INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	0	1	1
1	0	0	1	1	0 (discharge)
0	1	1	1	0	0 (discharge)
1	1	1	0	0	0 (discharge)

Default

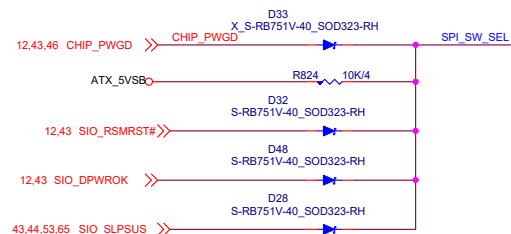
Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.

0825 Add D48, unstuff D33

For TL624 1.1

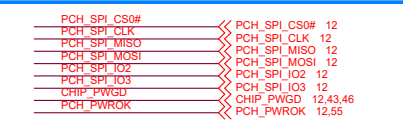
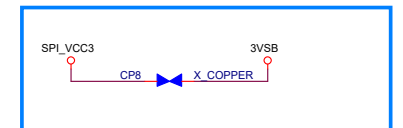
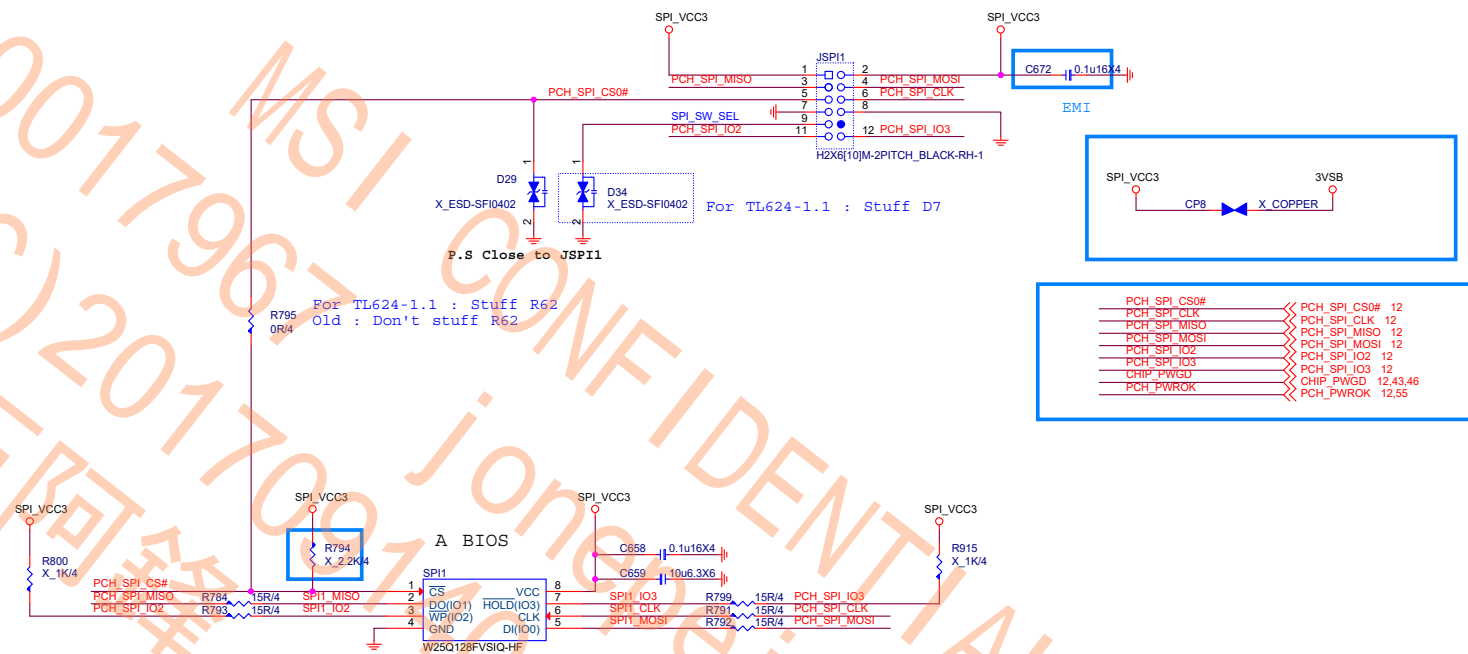


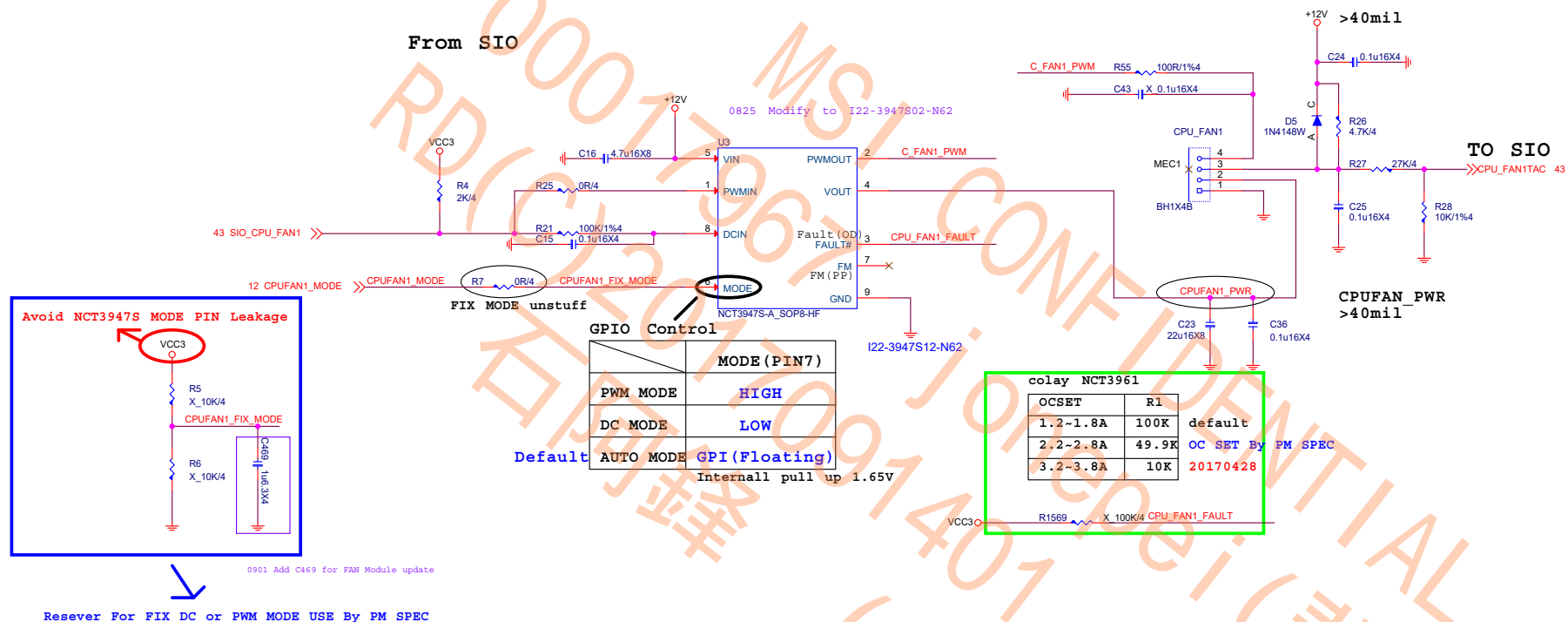
For TL624-1.1

SKYLAKE : Stuff D10/D17/R353

B85/H87 : Stuff D8/D9/R353

Others : Stuff R272





- 1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
- 2.FAULT : USE FAULT PIN Triger OVT/OC Protection,LOW Atcive (Reserve NEW IC)
- 3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)



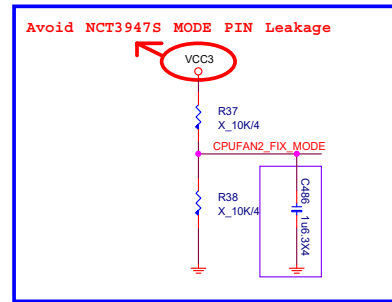
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MS-7B45

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Custom		CPU FAN1	20
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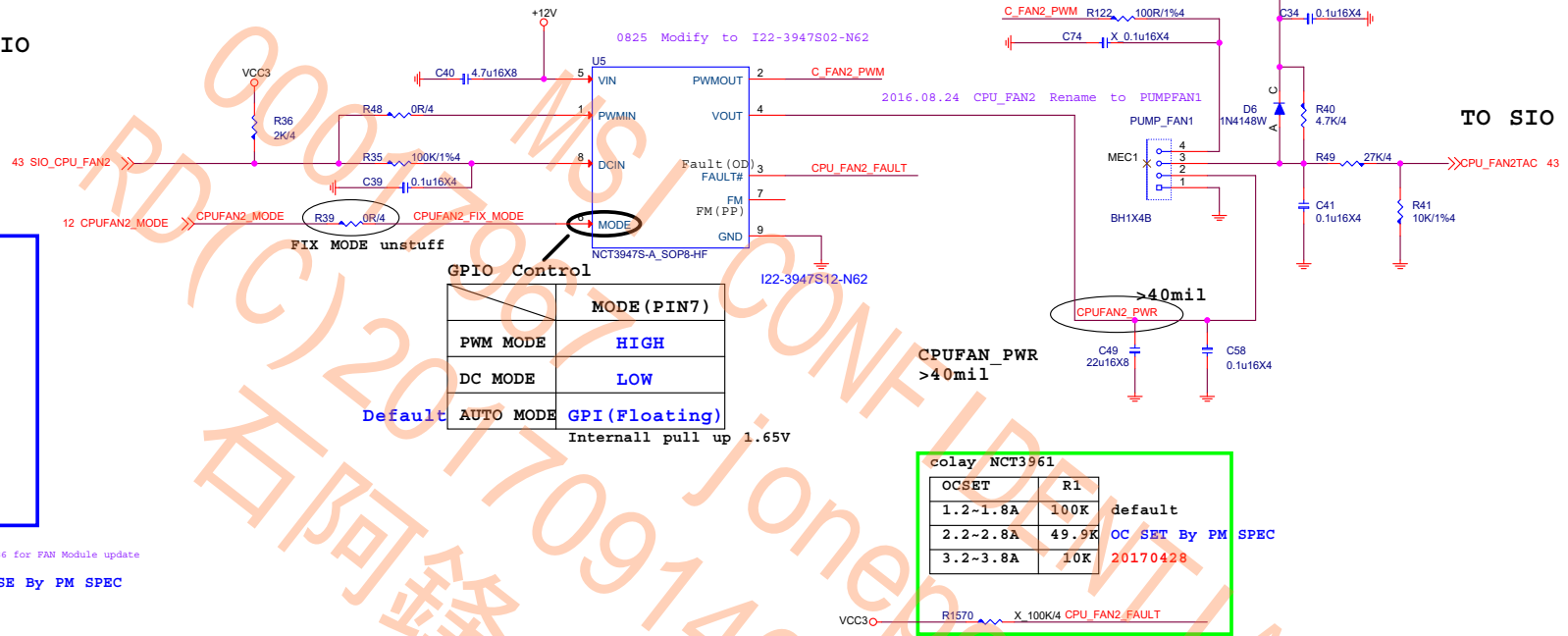
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

From SIO



0901 Add C486 for FAN Module update

Reserver For FIX DC or PWM MODE USE By PM SPEC



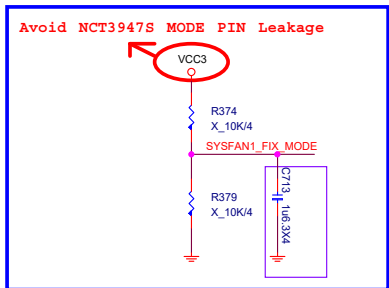
colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

VCC3-O R1570 X_100K/4 CPU_FAN2_FAULT

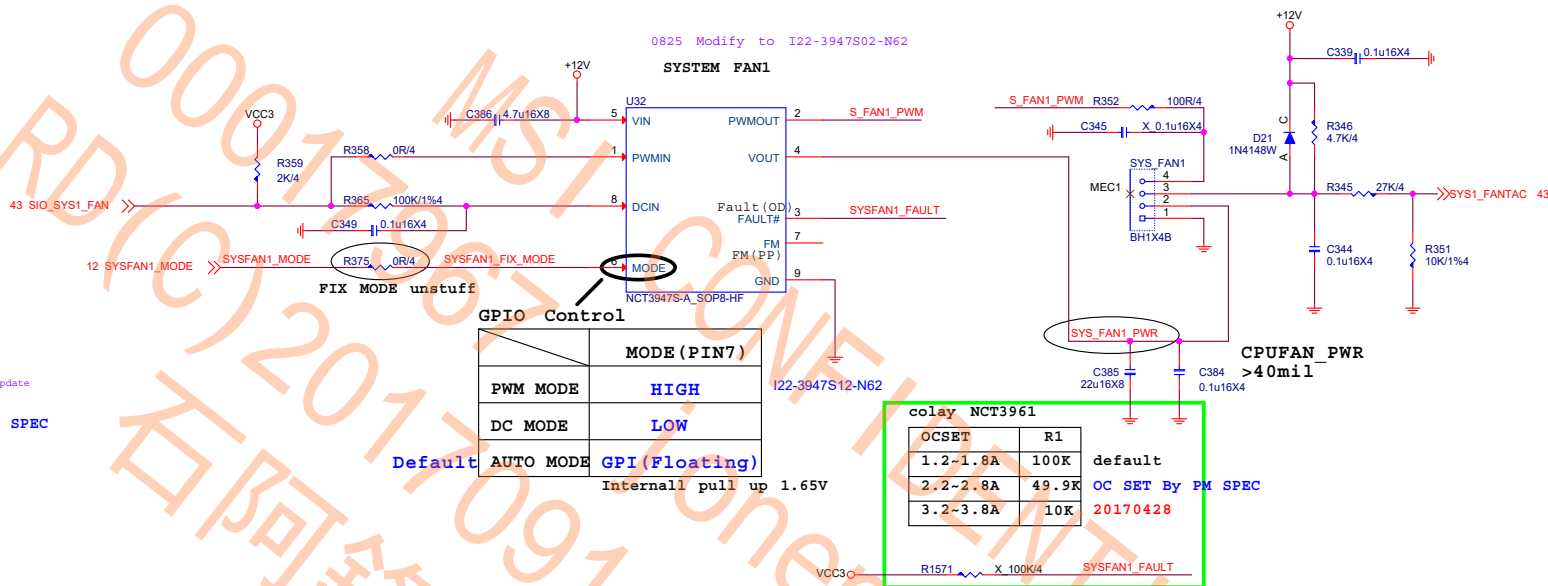
- 1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
- 2.FAULT : USE FAULT PIN Triger OVT/OC Protection,LOW Atcive (Reserve NEW IC)
- 3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

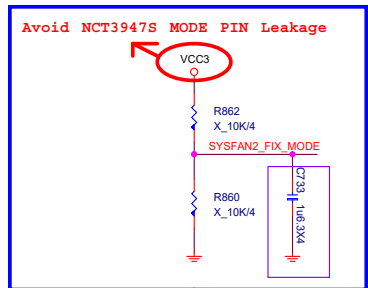


0901 Add C713 for FAN Module update

Resever For FIX DC or PWM MODE USE By PM SPEC

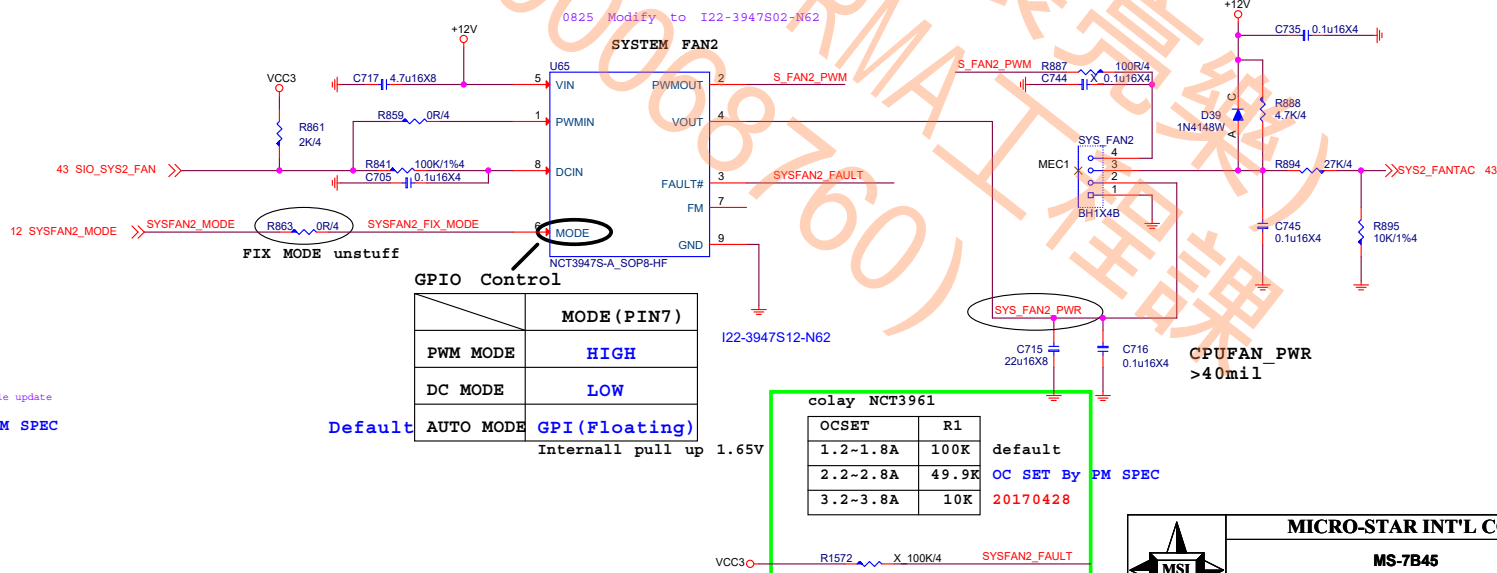


TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

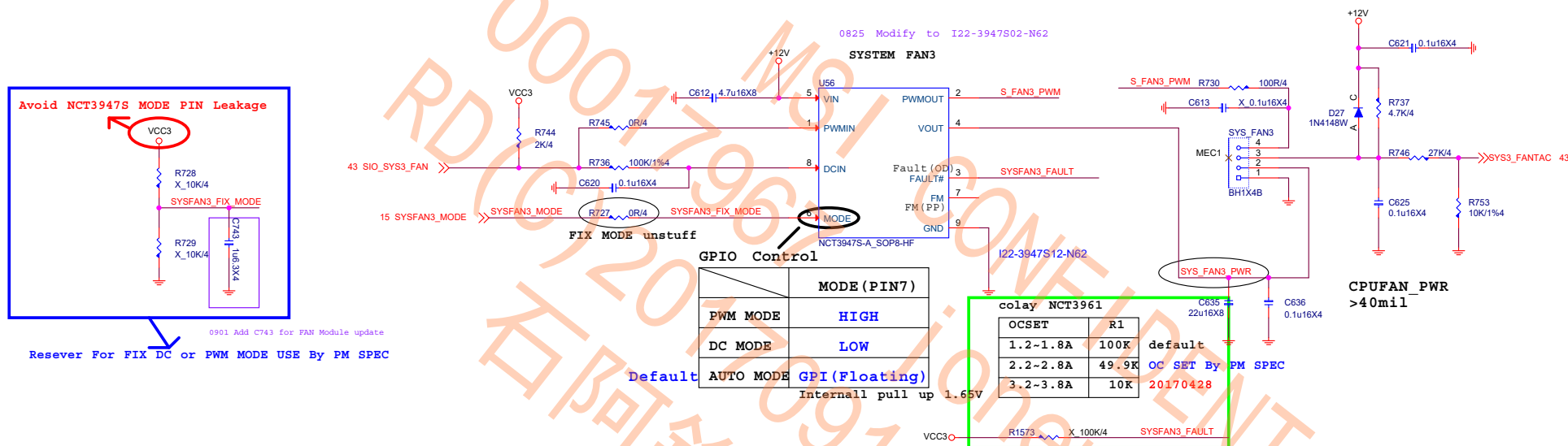


0901 Add C713 for FAN Module update

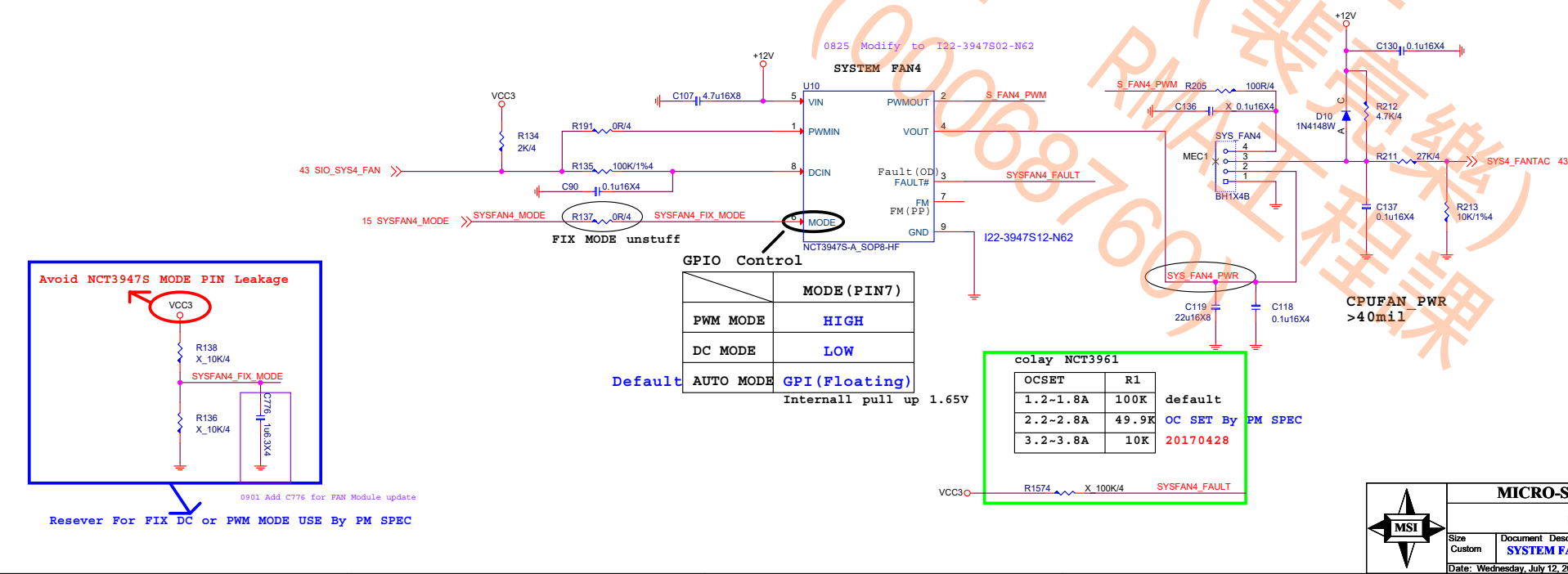
Resever For FIX DC or PWM MODE USE By PM SPEC



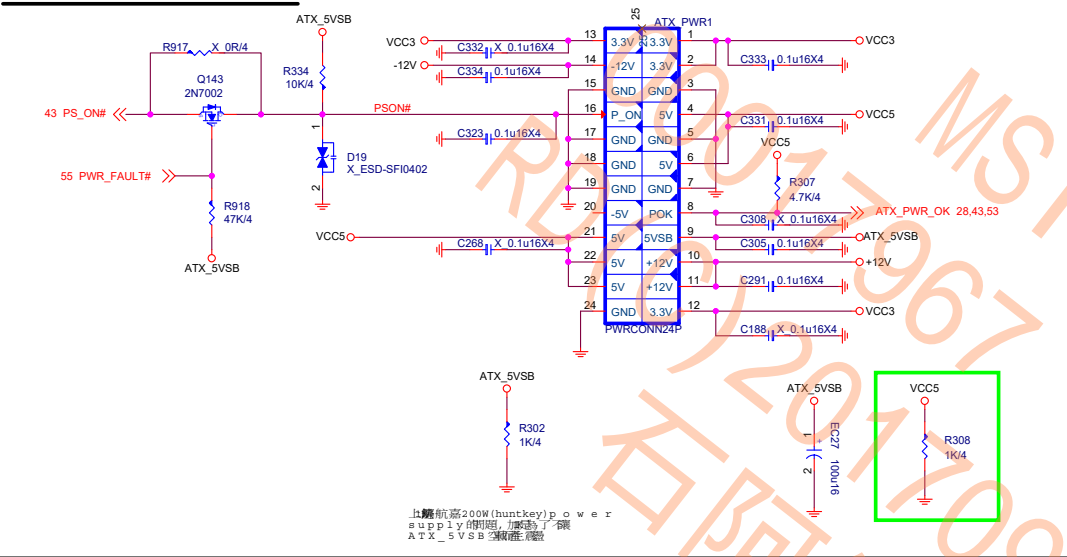
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



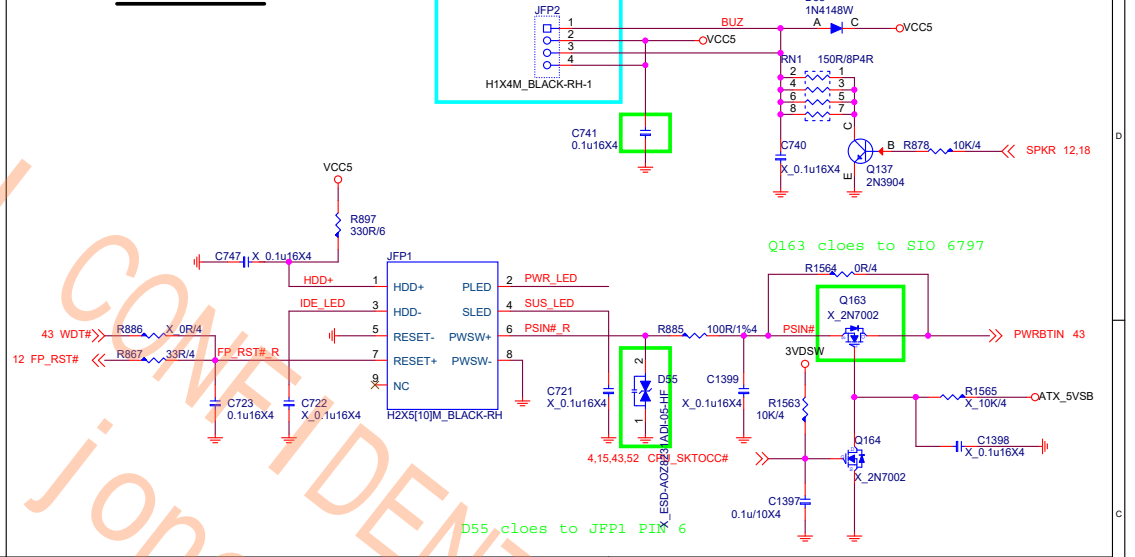
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



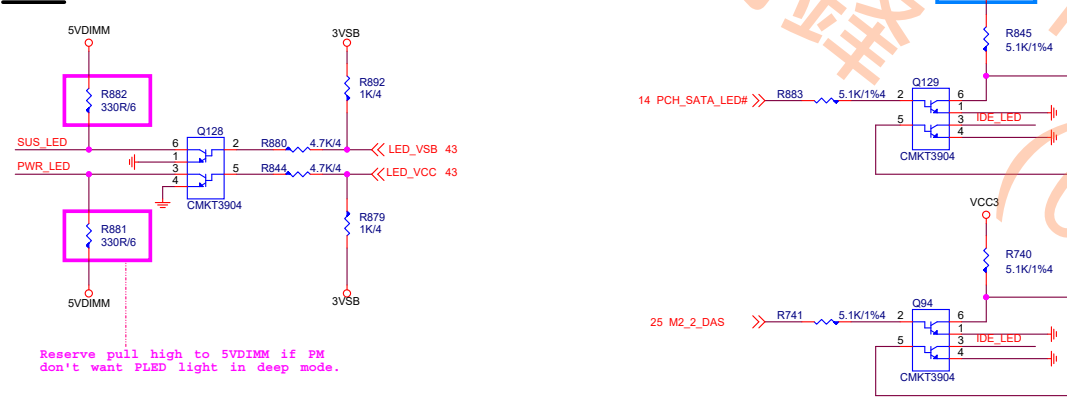
ATX POWER CONNECTOR



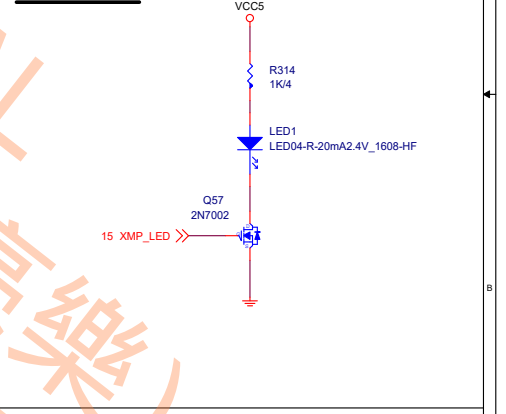
Front Panel



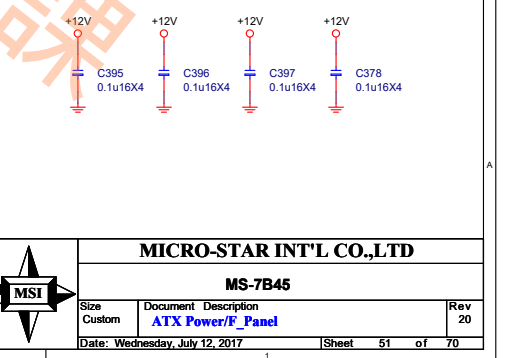
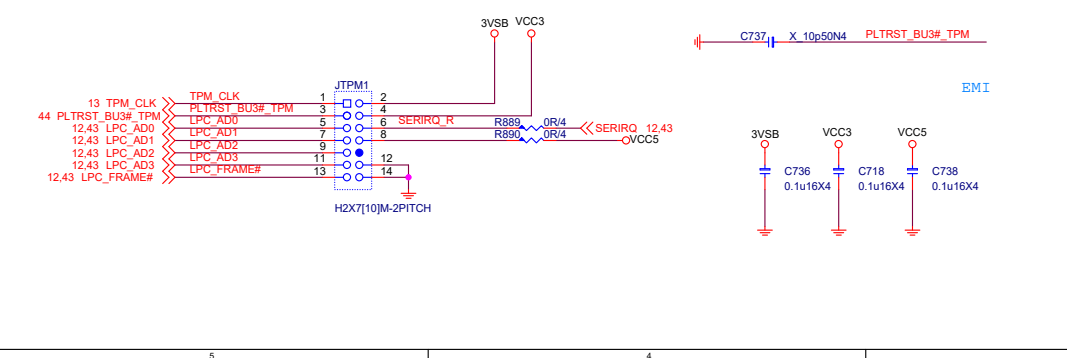
LED



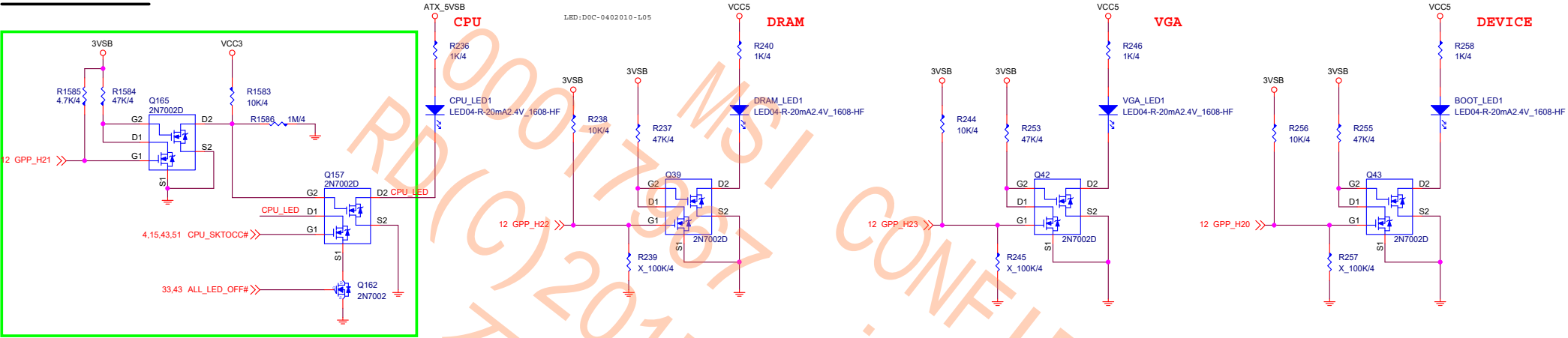
XMP LED



TPM Confirm ESPI TPM card and TPM card pin difine (Not ready)



EZ DEBUG LED

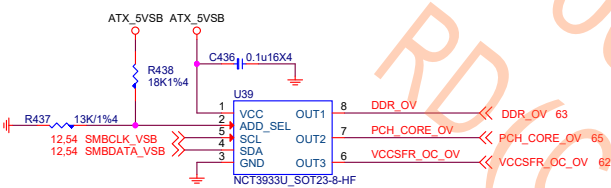


- 開機斷電狀態下，4個LED先維持 default 開機電：
1. 首先進行 CPU check CPU LED 亮，check PASS 後則 CPU LED 減掉。
 2. 接著依序進行 Memory / memory LED 亮 check PASS 後則 memory LED 減掉。
 3. VGA 的 check/VGA LED 亮，check PASS 後則 VGA LED 減掉。
 4. 因此最後正常順利開機後，三個 LED 減掉。
- (系統重啟或其他原因造成系統重開機則 LED 進行動作)

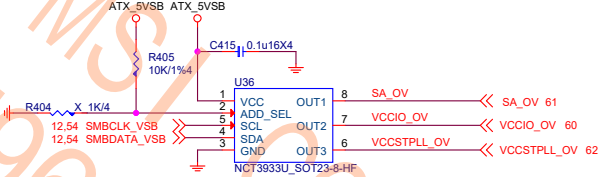
LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



0x20:RH=10K,RL=OPEN

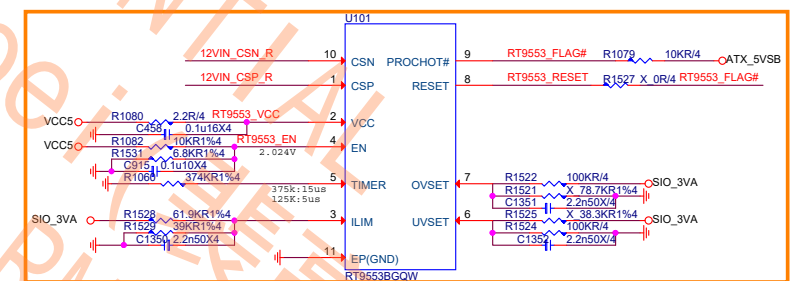
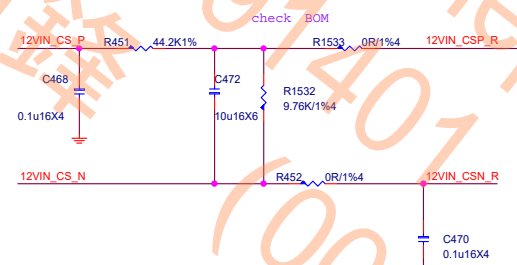
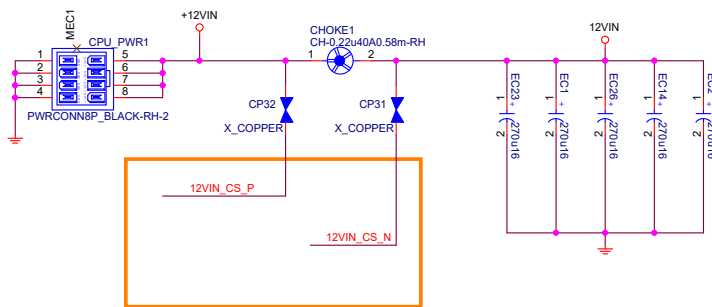
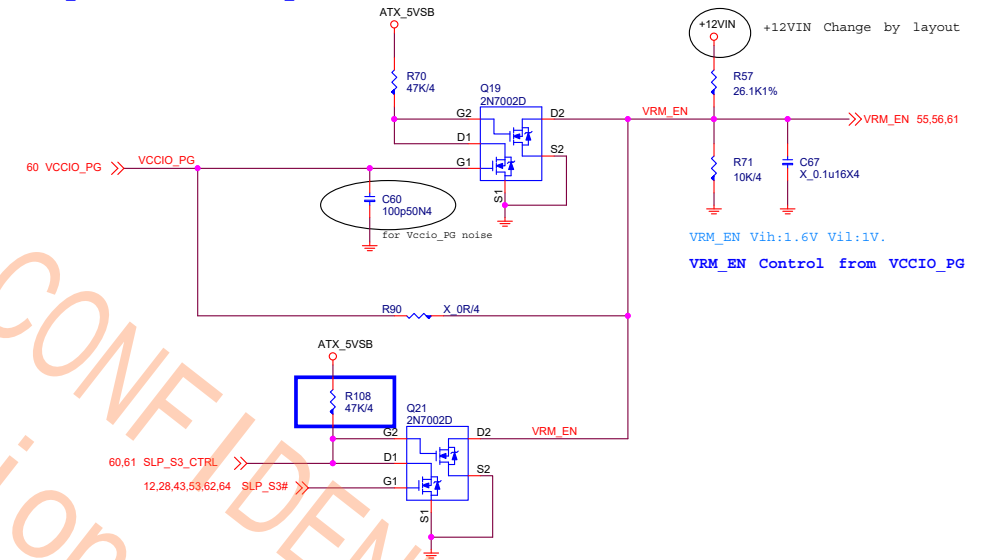
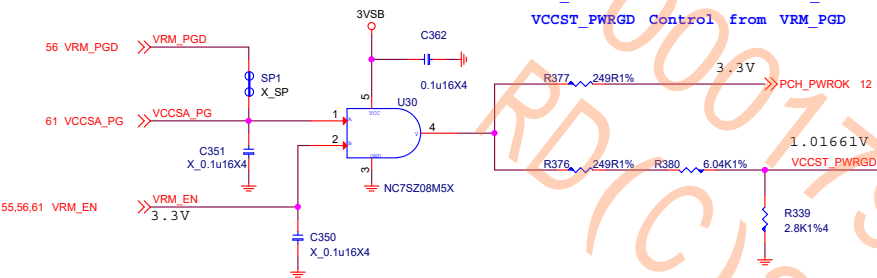


ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.

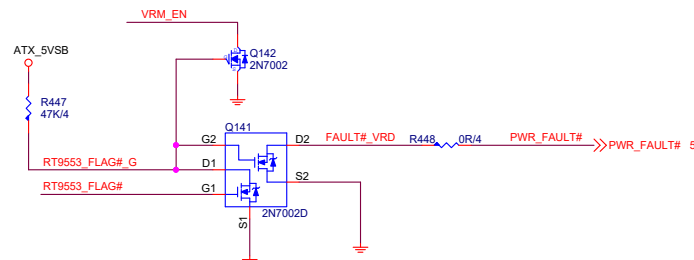
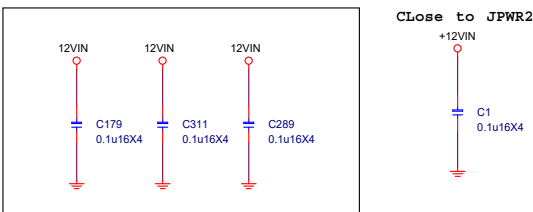
PCH_PWROK Control from VCCIO_PG&VCCSA
VCCST_PWRGD Control from VRM_PGD

VRM_EN Control from VCCIO_PG



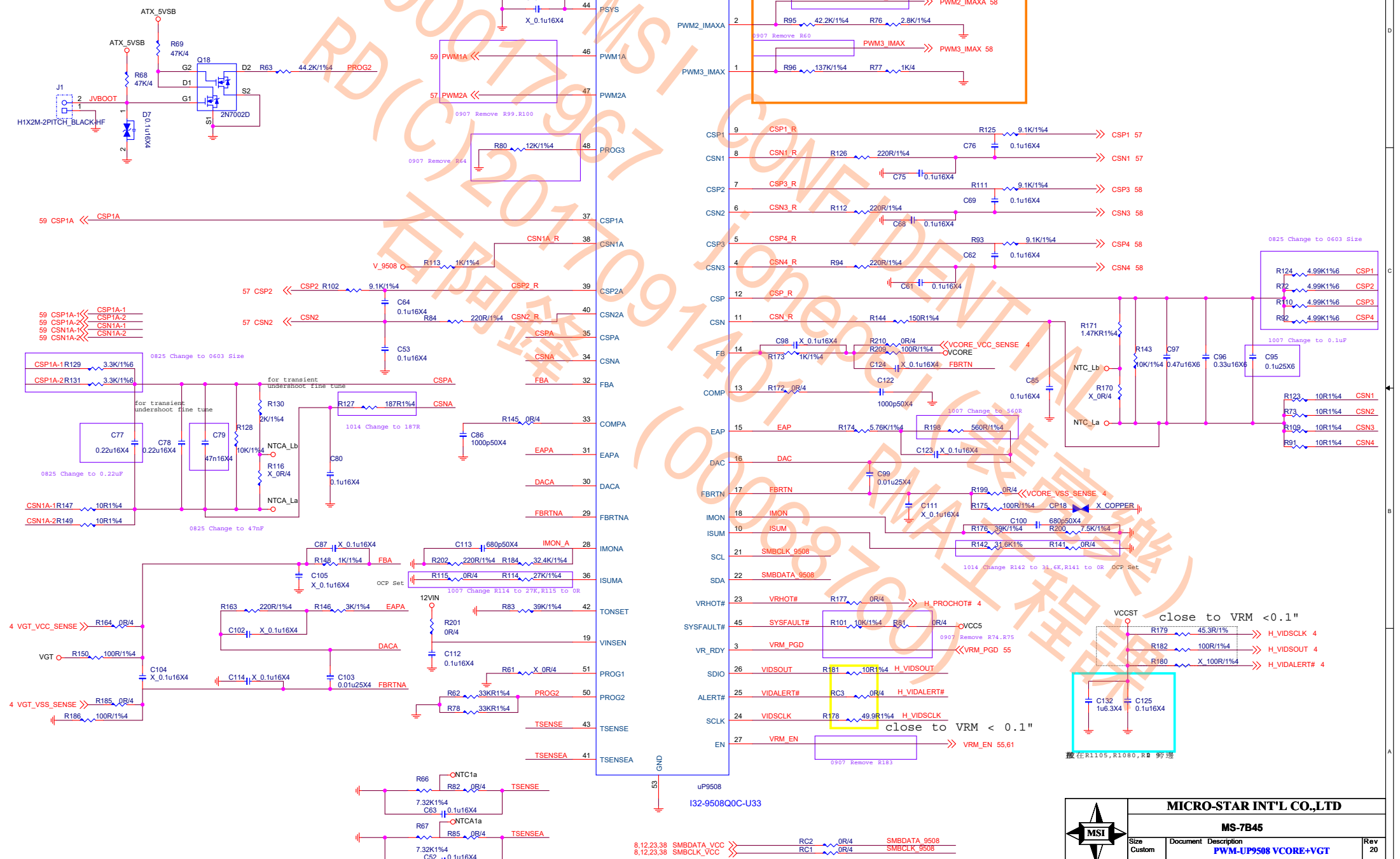
OCP:30A
Real OCP:30.05A
R17+R18>100k V_{sio_3va}= 3.38V Rdcr= 0.5 mohm

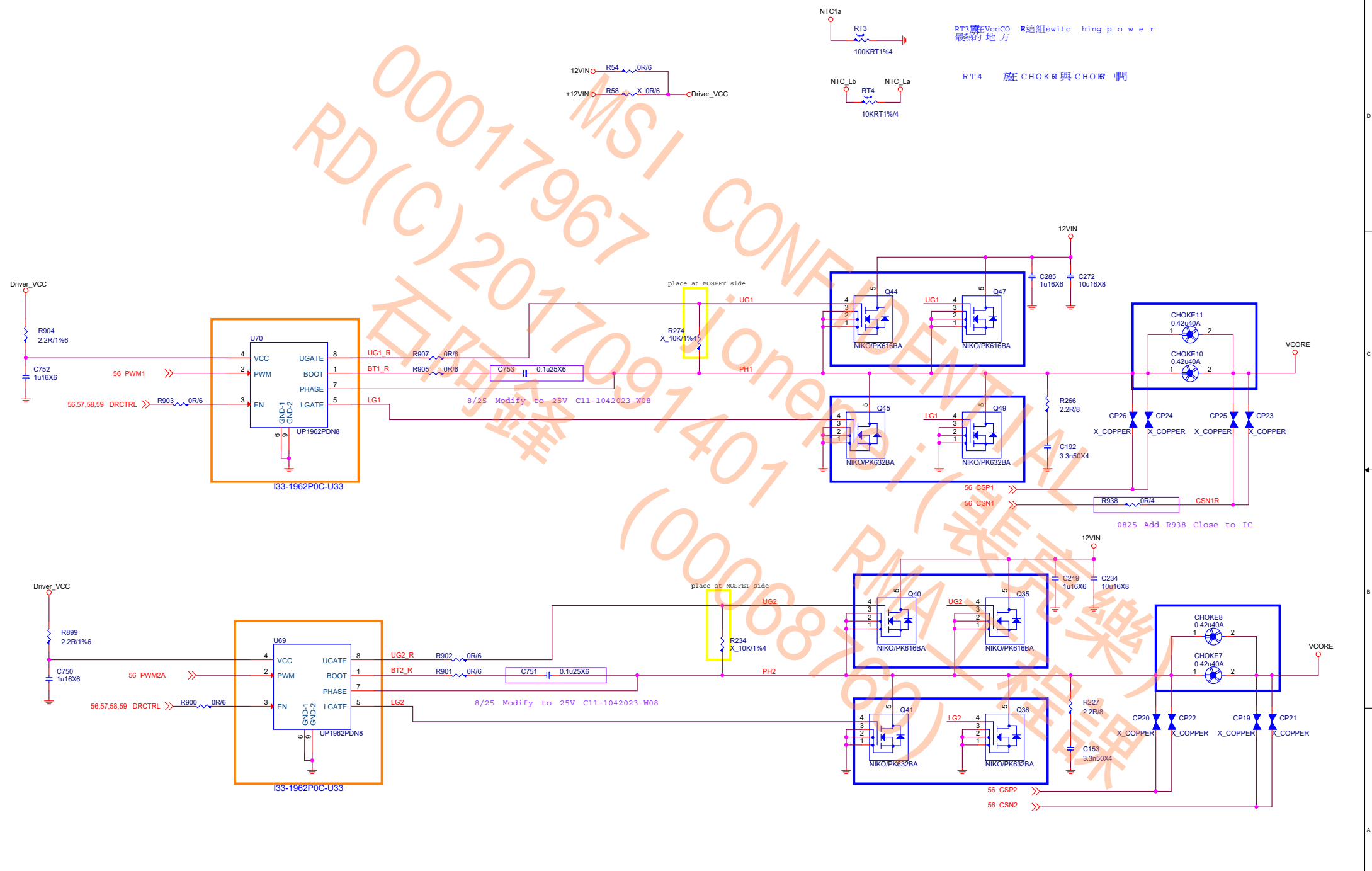
$I_{3933_imon} * [R17 * R18 / (R17 + R18)] = I_{step} * Rdcr * 100$
 $I_{3933_imon} = 10\mu A / step$
 $I_{step} = 4.968A$



Vcore: ICC Max 100A
LL: 2.1 mohm
OCP: 200A

VGT: ICC Max 48A
LL: 3.1 mohm
OCP: 75A





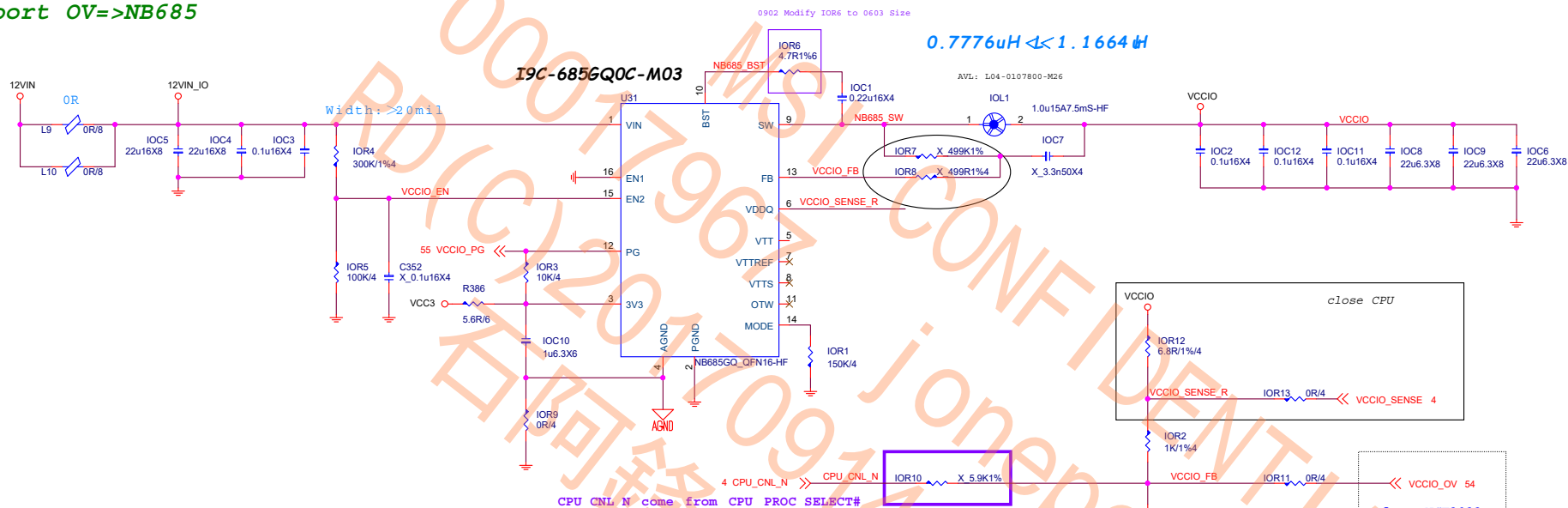
RT3 放在VccCO 最終付地方
RT4 旋 CHOKER與CHOSE 欄

VCCIO

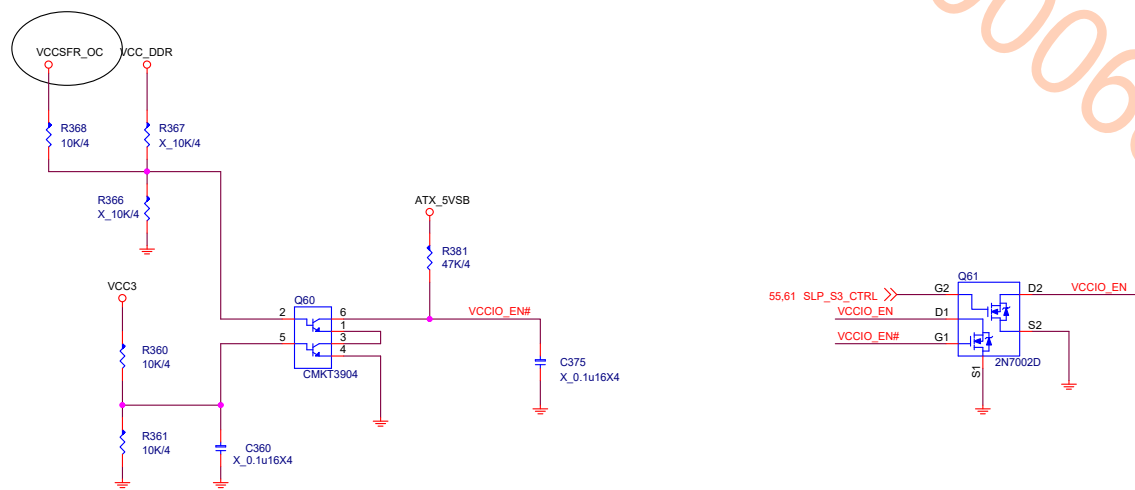
0.95V; 5.5A

support OV=>NB685

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.



SLP_S3# assertion to VCCIO VR disabled <1uS.
SLP_S3# assertion to VCC, VCCGT, VCCIO and
VCCSA rails completely off. <500ms



SLP_S3# assertion to VR disabled
max:1us

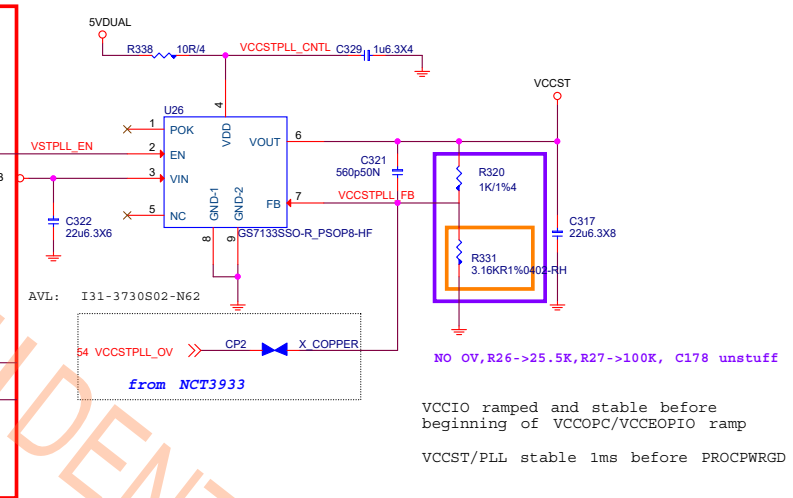
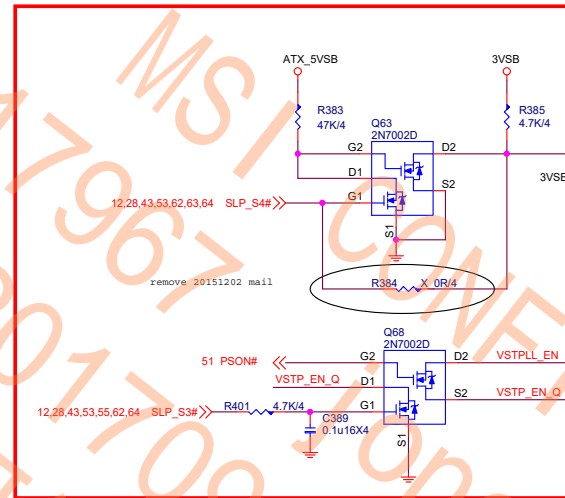
VCCST

VCCST:60mA
VCCPLL:150mA

1.05V; 210mA

For Cost down VCCST&VCCPLL merge

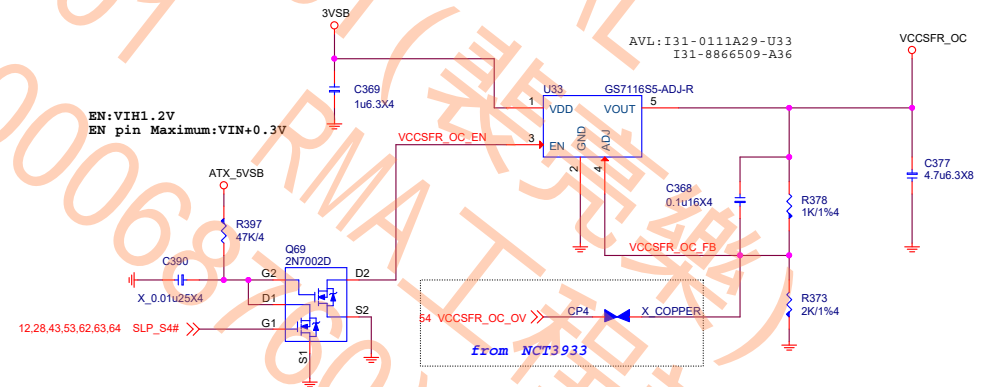
for Gaming3/5, Classic, ECO
and H110



VCCPLL OC

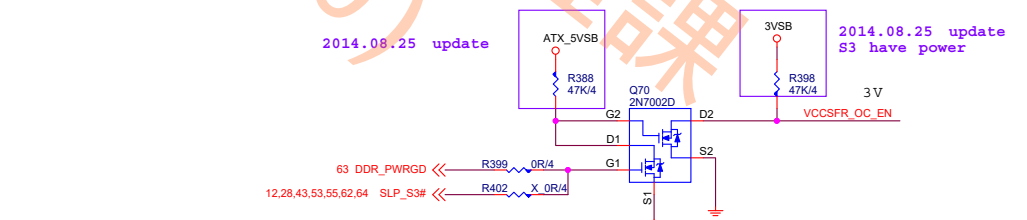
2014.08.21 update

1.2V; 130mA



2014.08.25 update

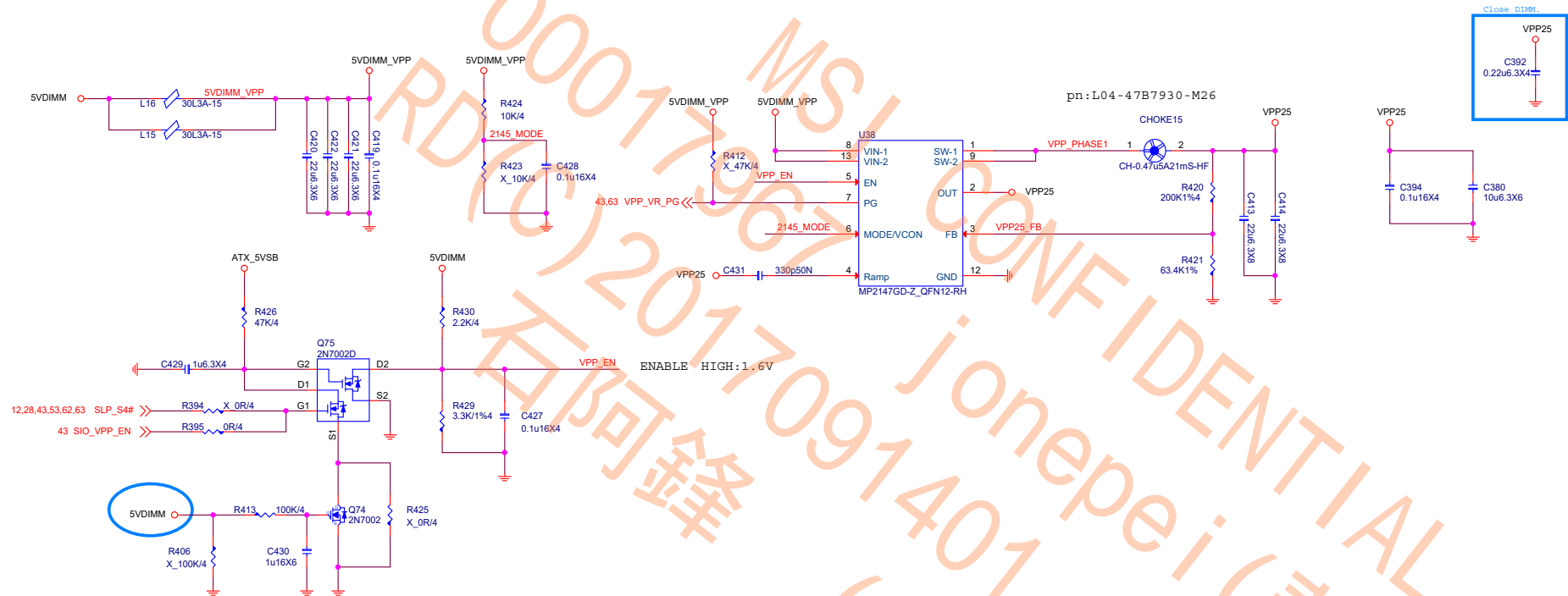
2014.08.25 update
S3 have power





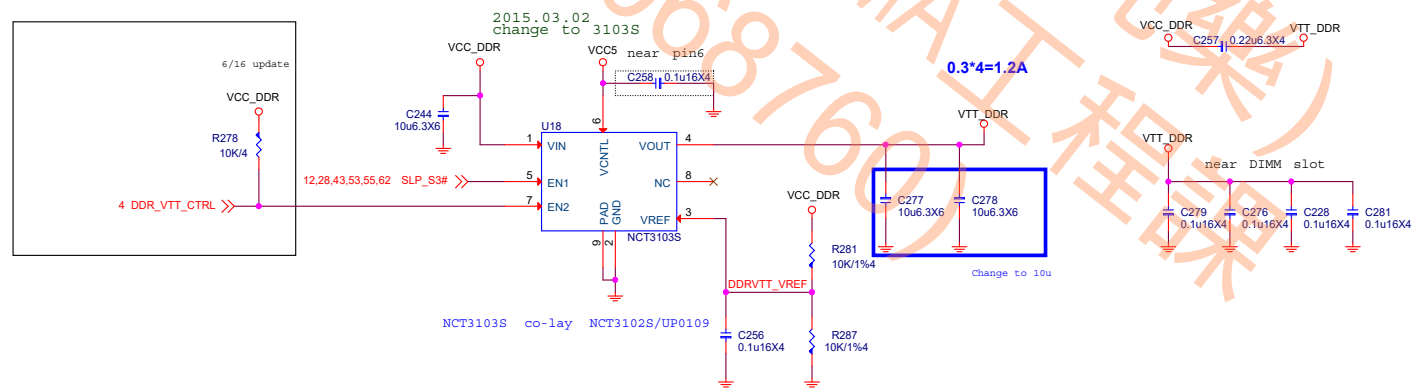
4DIMM :2.24A FOR DDR VPP2.5V

VPP25 Power
2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

DDR VTT Power



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Size Custom	Document Description DDR4 Power-VPP25	Rev 20
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PCH 1VSB

1.0V; 11.83A

OCP = 17.745A

Rocset = $1.5 * I_{max} * R_{dson}(low) / I_{ocset}$
 = $1.5 * 11.83 * 4.6mohm / 10uA$
 = 8.16K

Rocs: 7.87K, OCP:
 D03-4C05N03-O05 : 15.74A
 D03-632BA0C-N03 : 17.1A
 use UBIQ MOS need Check

Rdson(low) 4.5V

D03-3116M00-U47 : 3.6 mohm
 D03-632BA0C-N03 : 4.6mohm
 D03-3056M00-U47 : 6.2mohm

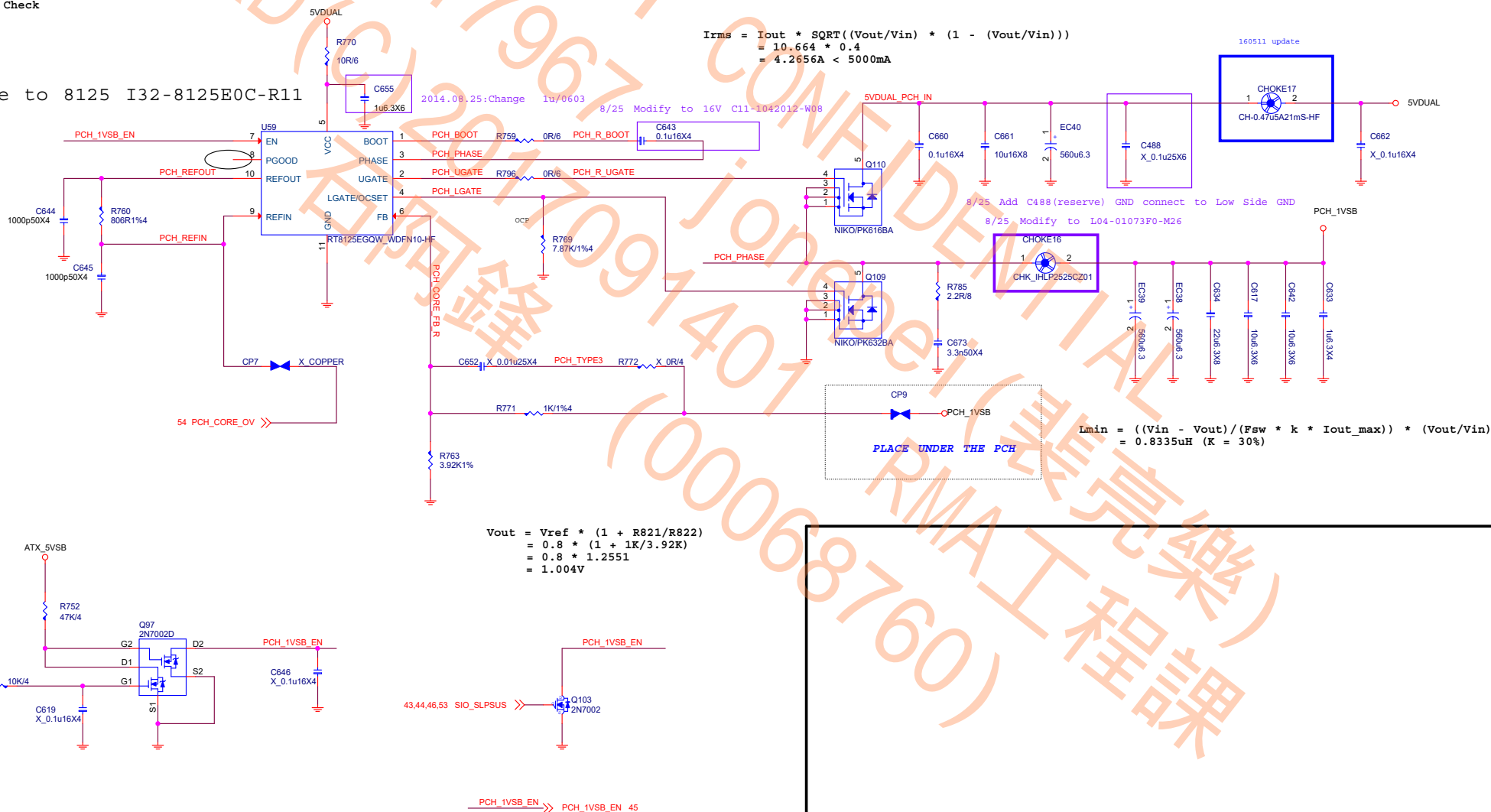
1504 change to 8125 I32-8125E0C-R11

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

160511 update



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Custom		PCH Core Power-RT8125	20
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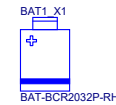
PCB



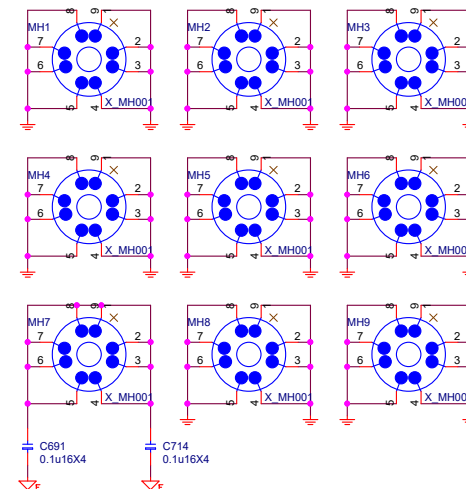
PD0-07A6311-G37
PD0-07A6311-E48



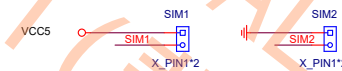
Audio Small Cover



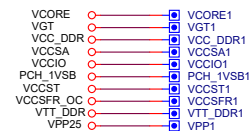
Mounting Holes



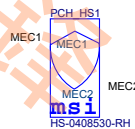
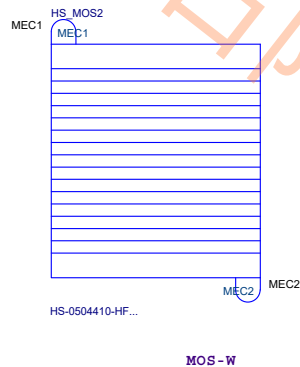
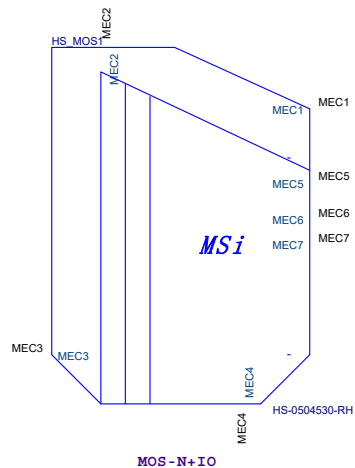
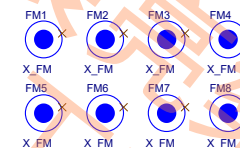
Simulation



Test point



Optical Fiducial Marks-120



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Custom	Manual parts		20
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